Enabling Resource-efficient AIoT System with Cross-level Optimization: A survey

Sicong Liu, *Member, IEEE,* Bin Guo*, *Senior Member, IEEE,* Cheng Fang, Ziqi Wang, Shiyan Luo, Zimu Zhou, *Member, IEEE,* Zhiwen Yu, *Senior Member, IEEE*

***Abstract*—The emerging field of artificial intelligence of things (AIoT, *AI+IoT*) is driven by the widespread use of intelligent infrastructures and the impressive success of deep learning (DL). With the deployment of DL on various intelligent infrastructures featuring rich sensors and weak DL computing capabilities, a diverse range of AIoT applications has become possible. However, DL models are notoriously resource-intensive. Existing research strives to realize near-/realtime inference of AIoT live data and low-cost training using AIoT datasets on resource-scare infrastructures. Accordingly, the accuracy and responsiveness of DL models are bounded by resource availability. To this end, the algorithm-system co-design that jointly optimizes the *resource-friendly DL models* and *model-adaptive system scheduling* improves the runtime resource availability and thus pushes the performance boundary set by the standalone level. Unlike previous surveys on resource-friendly DL models or hand-crafted DL compilers/frameworks with partially fine-tuned components, this survey aims to provide a broader optimization space for more free resource-performance tradeoffs. The cross-level optimization landscape involves various granularity, including the DL model, computation graph, operator, memory schedule, and hardware instructor in both on-device and distributed paradigms. Furthermore, due to the dynamic nature of AIoT context, which includes heterogeneous hardware, agnostic sensing data, varying user-specified performance demands, and resource constraints, this survey explores the context-aware inter-/intra-device controllers for automatic cross-level adaptation. Additionally, we identify some potential directions for resource-efficient AIoT systems. By consolidating problems and techniques scattered over diverse levels, we aim to help readers understand their connections and stimulate further discussions.**

***Index Terms*—Resource-efficient AIoT system, cross-level optimization, DL inference and training tasks**

I. Introduction

The Artificial Internet of Things (AIoT), also known as *AI+IoT*, was coined in 2017 and quickly gained widespread attention [1]. On the one hand, the rapid development of deep learning (DL) has led to the emergence of numerous intelligent services. On the other hand, the richer sensors and enhanced DL computing capabilities of intelligent infrastructures have given rise to a new category of devices known as *AIoT devices*. AIoT devices are distinct from traditional IoT sensor nodes due to their broader range of sensing capabilities, ability to perform complex computations directly on the device, and greater connectivity capabilities.

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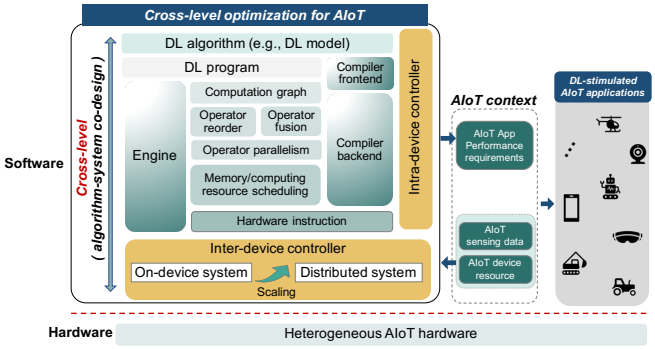


Fig. 1: Illustration of cross-level optimization for the resource-efficient AIoT system, spanning the resource-friendly algorithm, model-adaptive system scheduling, to context-aware intra-/inter-device controllers.

Moreover, there is a growing trend to integrate DL-powered intelligence into tiny embedded AIoT devices for two primary reasons. *First*, the proliferation of AIoT devices has resulted in a massive increase in distributed sensing data captured in various modalities [2]. By executing DL inference and training tasks on resource-scarce AIoT devices, rather than transmitting data to remote centers, *e.g.*, cloud, like traditional IoT, we can save bandwidth and latency while guaranteeing recognition accuracy. *Second*, AIoT applications such as medical assistance and security monitoring collect sensitive user information, posing well-known privacy risks [3]. It is preferable to process data locally or at trusted nearby devices. However, modern DL models are notoriously resource-intensive, making it challenging to achieve real-time inference and low-cost training on resource-scarce AIoT devices.

Given these challenges, previous research has explored *resource-friendly DL models* and *resource scheduling* techniques, either individually or in combination. *First*, *resource-friendly DL model compression* have been widely investigated to reduce the resource demands of DL models at the algorithm level. They include standalone model compression techniques [4], [5], and automated neural architecture search (NAS) frameworks [6]–[8]. However, despite extensive research on model compression, compressed DL models typically compromise accuracy to reduce resource demands. *Second*, some *hand-crafted DL compilers/frameworks* fine-tune diverse system levels to reuse the input data and reduce runtime overhead. For example, TVM [9] optimizes DL operators at the computation graph level, Tensorflow

Runtime (TFRT) [10] implements efficient execution of the computing kernel, and TensorflowXLA [11] designs a linear algebra compiler engine for the TensorFlow framework. *Third*, algorithm-system co-design brings better performance. For example, MCUNet [12] co-designs the TinyNAS, for DL model design, and TinyEngine, for code compilation and memory scheduling. However, algorithm-system co-design is difficult for non-experts. And existing techniques only manually optimize partial system levels to provide a feasible solution.

To this end, providing a relatively complete picture of the cross-level optimization space is necessary. This can assist researchers in finding suitable technique combinations for their specific requirements more freely and help automated frameworks build a finer-grained search space to push the boundary of performance-resource tradeoffs. We summarize the cross-level optimization space as follows:

- *Resource-friendly algorithm level* is concerned with specifying DL models to balance performance and resource constraints. However, the accuracy of lightweight models is degraded and bounded by resource budgets.
- *Model-adaptive system scheduling level* comprises various fine-grained granularities, *e.g.*, computation graph, operator, memory, compiler, engine, and instructor. This level aims at utilizing hardware resources to their fullest capacity without compromising model accuracy.

Joint optimizing across these levels with bi-directional feedback can improve runtime resource availability and performance-resource tradeoff for AIoT. However, no existing surveys have extensively covered all of these levels. The most related previous surveys include [13]–[17]. *First*, many mobile and embedded DL surveys focus on resource-friendly model compression [13], [18] from the algorithm level. *Second*, surveys on edge computing [15], [16] spanning networking and computation offloading [14], [16], pay little attention to the distributed cross-level optimization, *e.g.*, data movement in partitioned computation graphs and memory allocation across devices at runtime. *Third*, [17] maps the DL computation to hardware. However, it targets DL-oriented compiler optimization, which does not co-design the DL models with compilers. This paper comprehensively analyzes the resource-efficient AIoT systems, covering all of these levels. As depicted in Figure 1, it not only encompasses optimization techniques used in stand-alone fields like on-device DL [19], distributed DL [20], [21], and tiny systems [22] but also expands the optimization possibility in the AIoT context.

In particular, the dynamic nature of AIoT context poses a significant challenge: how to adaptively optimize cross-level DL systems to meet varying application performance requirements while satisfying resource constraints. The *dynamic context* includes a range of factors, including heterogeneous AIoT resources, agnostic live data, varying user-specified performance demands, and device-imposed resource constraints. To address these challenges, the AIoT system should also contain context-aware controllers across these levels:

- *Intra-device cross-level controller* establishes a control flow across different system levels to automate the dynamic context awareness, optimization technique combination, and adaptive co-design loop.
- *Inter-device cross-level controller* judges the complementarity of distributed AIoT sensing data and resources, scaling cross-level systems between on-device and distributed schemes.

Therefore, we identify essential enabling technologies for diverse tasks. Each of them encompasses cross-layer optimization, but with different constraints.

- Cross-level optimization for On-device DL inference (§ III-A). It aims to achieve better real-time performance and higher accuracy by minimizing DL model redundancy and maximizing on-device resource capability.
- Cross-level optimization for Distributed DL inference (§ III-B). By aggregating more computing resources and sensing sources, it can further optimize latency and accuracy than the on-device scheme. It operates with a similar cross-level spectrum but utilizes distributed scheduling.
- Cross-level optimization for on-device DL training (§ IV-A). DL training is more complex than inference. It aims to reduce training costs and maintain accuracy.
- Cross-level optimization for distributed DL training (§ IV-B). It further coordinates data fusion and resource aggregation to optimize DL training efficacy and efficiency.
- Resource-efficient AIoT applications (§ V). The aforementioned techniques and systems stimulate a wide range of AIoT applications with flexibility and adaptivity.

In summary, the key contributions of this work can be summarized as follow:

- To the best of our knowledge, this is the first to describe the characteristics and architectures of the resource-efficient AIoT system exactly. It provides a *cross-level spectrum* of the system optimization space for AIoT.
- We propose a novel taxonomy of existing techniques, summarizing how state-of-the-art address issues across different levels of the resource-efficient AIoT system. Additionally, we demonstrate how context-aware controllers can automatically select cross-level techniques for AIoT.
- We discuss open issues in resource-efficient AIoT systems and suggest potential future research directions.

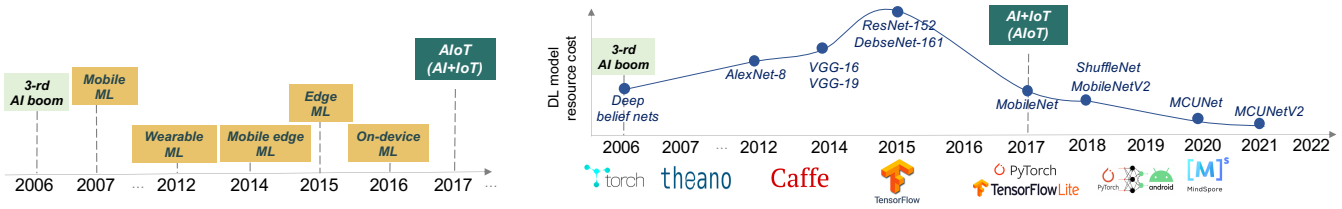
This section introduces the background and leads to the motivation for this survey. In the rest of this paper, we present fundamentals of the resource-efficient AIoT system in § II, introduce the enabling techniques across diverse levels for DL inference and training tasks in § III and § IV, respectively. And then, we list related AIoT systems and applications in § V. Finally, we discuss the open issues in § VI and conclude this paper in § VII.

II. Fundamentals of Resource-efficient AIoT system

This section presents an overview of the resource-efficient AIoT system, departing from existing related areas.

A. AIoT Paradigms

Artificial Intelligence of Things (AIoT) refers to the integration of artificial intelligence (AI) technologies with Internet



(a) Development of related areas

(b) Development of DL models (a showcase of vision fields) and frameworks

Fig. 2: Illustration of various related areas and frameworks.

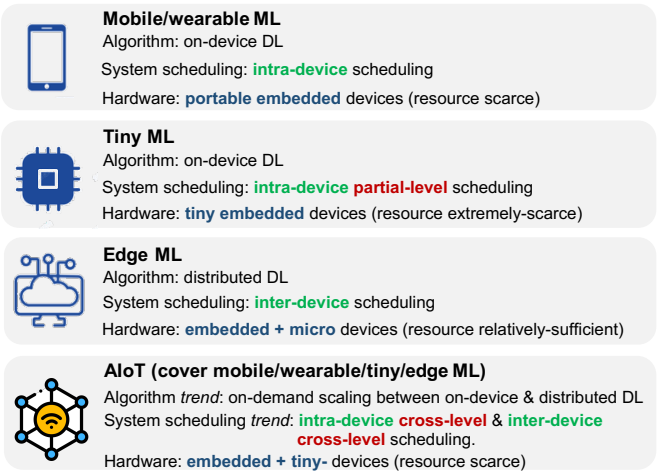


Fig. 3: Difference of related paradigms.

of Things (IoT) infrastructures to improve data analytics [23]. The primary computational task in the resource-efficient AIoT system is *data analysis*. As depicted in Figure 2, deep learning (DL) has emerged as the dominant AI methodology for learning and analyzing data since the third AI boom [24]. And there is a growing trend to incorporate DL-powered intelligence into tiny embedded AIoT devices with the advancement of embedded hardware and on-device DL technologies [25]. In addition, new development frameworks have been launched specifically targeting embedded devices, such as TensorFlow Lite [26], Caffe2 [27], and Pytorch Mobile [28], in order to promote DL-based AIoT applications.

Several related areas utilize overlapping enabling techniques but have varying focuses, as shown in Figure 2a and Figure 3. We differentiate them below.

1) Mobile [29] and *Wearable ML* [30] focus on mobile data analytic patterns and application experience (*e.g.*, real-time response) on *portable embedded* mobiles and wearables.

2) Tiny ML [31] concerns machine learning aware architectures, frameworks, techniques, tools, and approaches which are capable of performing on-device analytics at *tiny embedded* devices with extremely limited resources, *e.g.*, Microprogrammed control unit (MCU). And TinyML project [32] aims to improve the efficiency of systems by requiring less computation, fewer engineers, and fewer data to facilitate the giant market of tiny embedded applications. It covers the management of data and the deployment of models.

3) Edge ML presents to keep data near where it's generated, avoiding costly and privacy-threatening data transfers [33]. Instead of shipping data centrally to perform data analytics, edge computing analyzes data using ML at the edge while maintaining accuracy and latency. The edge includes embedded and micro devices with relatively sufficient resources.

As these related areas evolve, many enabling techniques and frameworks can facilitate AIoT from different aspects. Techniques such as DL models for mobile and edge computing [30] and on-device/distributed DL deployment [29], [33] provide various model compression and offloading algorithms for inference and training. Frameworks such as TFlite [26], CMix-NN [34], TVM [9], TensorFlow XLA [11], and oneDNN [35] offer a range of acceleration options and memory scheduling support for DL. The key distinction lies in the AIoT system's ability to integrate these technologies in a novel, context-aware and cross-level manner. Specifically, we define some important concepts as follows:

AIoT computing task and paradigm. *AIoT data* mainly includes two types, *i.e.*, *live sensing data* and accumulated *dataset*. And their analysis is concentrated in two stages, *i.e.*, DL *inference* and *training*, respectively.

- *Near-/realtime inference of AIoT live data on resource-scare AIoT devices*. The AIoT *live data* are sensed by distributed AIoT devices and should be analyzed fastly.
- *Low-cost training using AIoT dataset on resource-scare AIoT devices*. The AIoT *dataset* are sensed and held by distributed AIoT devices and should be consumed with low data transmission and training costs, *e.g.*, memory.

Alternatively, inference and training tasks can be performed on-device or at distributed edges within the networked system, which enable a plethora of innovative AIoT applications that go beyond the conventional IoT paradigm in terms of accuracy, latency, bandwidth, privacy, and energy efficiency [1].

AIoT devices refer to intelligent end/edge devices equipped with advanced sensors and DL computing capabilities. This category includes mobiles, wearables, robots, drones, and other physical devices. In this context, the "end" device serves as the primary sensing source. Similarly to edge computing, the "edge" refers to devices located between the sensing data source and the cloud center path. In the realm of AIoT, there is a preference for prioritizing physically nearby edge devices to enable cost-effective near-sensing-data computing.

Resource-efficient AIoT system. Unlike software-hardware co-design approaches [36], [37], our focus is on the system software, specifically the ***algorithm-system co-design***. This approach allows for effective utilization of existing hardware

resources in dynamic AIoT contexts. AIoT applications like smart home and smart retail rely on a plethora of AIoT devices equipped with advanced sensors and embedded processors. Replacing these devices with newer hardware can often be costly and impractical. Therefore, adopting a strategy that optimizes the usage of available hardware resources can be an efficient and cost-effective solution in such scenarios. We refer to the DL-based system on AIoT devices as ***resource-efficient AIoT system*** in the following part for short. The resource-efficient AIoT system is responsible for distributing and federating AIoT sensing data analytics across resource-constrained and heterogeneous end/edge devices for DL inference and training. It is worth noting that communication networking for AIoT is outside the scope of this survey.

B. Cross-level Characteristics of AIoT System

We provide an overview of the remarkable cross-level characteristics and architectures of resource-efficient AIoT systems. As illustrated in Figure 4, the resource-efficient AIoT system comprises two key levels: the *resource-friendly algorithm* and *model-adaptive system scheduling*. These levels should be *co-designed* to ensure coherent resource usage. We outline their specific features and functionality below.

1) Resource-friendly algorithm level: dynamically scalable, divisible, and composable DL models. The DL models for AIoT should be *dynamically scalable, divisible, and composable* in both DL inference and training tasks. *First*, the DL model (*e.g.*, structure, parameter size) should be *scalable* with diverse compression degree to satisfy the platform-imposed dynamic resource constraints (*i.e.*, memory, computing, and battery) and application-specified performance demands (*i.e.*, accuracy, latency, energy cost). This scheme will inevitably bring accuracy fluctuations if the DL models are poorly designed. *Second*, DL models' divisible and composable properties are necessary to offload computation to distributed AIoT devices. Particularly, the divisibility of DL models depends on the internal dependency of DL layers, channels, and operators. And the composable property of DL models is able to adjust the system to offload different DL block combinations to diverse AIoT devices for dynamic resource availability.

2) Model-adaptive system scheduling level: maximizing runtime hardware capability. This level aims to utilize hardware resources to their fullest capacity without compromising model accuracy. Even for identical DL model configurations, mapping different model layers/operators onto diverse memory units in varying sequences results in different latency and resource overhead [9], [38], [39]. For example, integrating the memory fragmentation in the tensor layout of SqueezeNet can reduce 42% wasted memory fragmentation [40]. Therefore, designing appropriate strategies at computation graph, operator, and memory allocation levels to cater to the upper-level models can enhance runtime resource availability. Notably, this level can *iteratively allow a more flexible DL model design space for the algorithm level, thereby pushing the limitations on accuracy-resource trade-offs*.

3) Intra-device controller: automating the adaptive on-device cross-level optimization. The efficacy of various optimization techniques at different levels can vary for the same

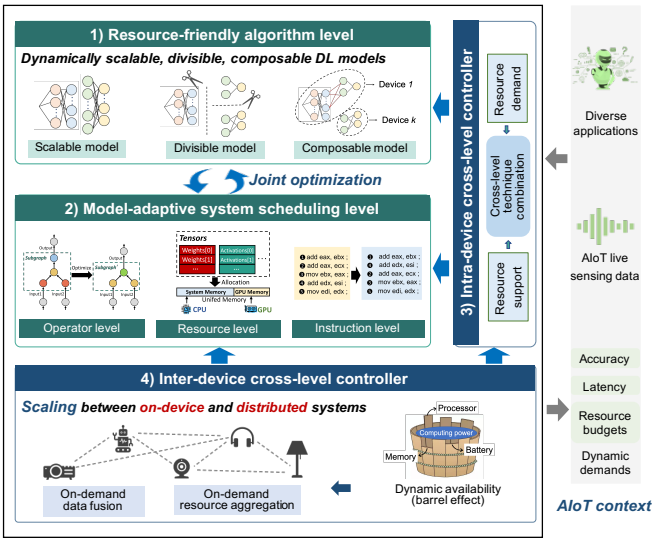


Fig. 4: Resource-efficient AIoT system architecture, involving two joint-optimized levels and two context-aware controllers.

DL model. And even within the same level of optimization techniques, there can be differences in their performance. As a result, it is imperative to develop an extra control flow to automate the adaptive optimization of DL models and system scheduling in a cross-level manner. Also, adaptively adjusting the cross-level techniques based on dynamic contexts, such as input data, resource availability, and user demands, is necessary. The controller monitors the *resource availability* of the target platforms and predicts the *resource requirements* of the AIoT system based on the current model configurations and scheduling strategies. The controller automatically adjusts techniques across different levels if the resource demand exceeds the supply or does not align with the user-defined budgets.

4) Inter-device controller: automating the adaptive distributed cross-level optimization. It scales the cross-level AIoT system from on-device to distributed schemes for achieving better performance-resource efficiency trade-off. As shown in Figure 5, the distributed AIoT devices collaborate on demand for two motivations:

- ***On-demand sensing source association***. With the proliferation of data-rich sensors (*e.g.*, cameras, LIDAR, and hyperspectral imagers), different distributed sensing sources have temporal connections for specific DL training/inference tasks. Distributed multi-modal data benefit the environment/object recognization from different vantage points with various physical properties [41]–[44]. The inter-device controller needs balance the necessity of sensing source association within the networked system to the accuracy of AIoT tasks and the overhead.
- ***On-demand computing resource aggregation***. As mentioned above, AIoT prioritizes the on-device scheme, followed by the distributed collaboration scheme with nearby edges, to realize near-sensing-data computing for saving transmission bandwidth and protecting data privacy [45], [46]. Executing DL models requires large computing/memory resources that are not always avail-

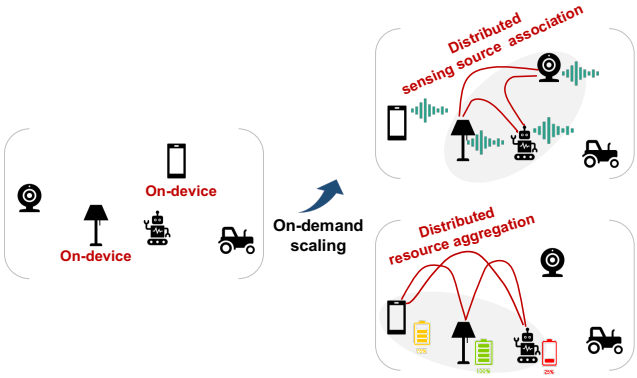


Fig. 5: The inter-device controller scales the cross-level AIoT system between on-device and distributed schemes for on-demand sensing source association or resource aggregation.

able in a single AIoT device, significantly when the scale and complexity of DL models continuously increase. Scheduling the most suitable distributed devices within locally connected and resource-constrained edge clusters is necessary yet challenging [47], [48].

C. Taxonomy of Enabling Techniques

We identify the following essential enabling technologies for resource-efficient AIoT systems, considering the cross-level deployment issues mentioned earlier. Figure 6 summarizes our taxonomy, *i.e.*, cross-level optimization for both resource-efficient *DL inference and training tasks*.

1) Cross-level Optimization for DL Inference Tasks: There is a growing trend today to bring DL-powered intelligence into AIoT devices for various applications, *e.g.*, object recognition [49]–[52], semantic segmentation [53]–[55], object tracking [56]–[58], natural language processing [59], [59], [60], and recommendation [61]–[63].

Challenges. It is non-trivial to achieve near-/real-time DL inference with limited resources in AIoT devices, which is critical for AIoT live data to satisfy the applications' responsiveness. First, on-device DL inference benefits user privacy and robustness. However, mainstream DL models, such as Zero-DCE for low-light video enhancement [64], are still computation-intensive and fail to achieve real-time processing on the local AIoT device. Second, distributed DL inference strives to satisfy stringent demands across multiple dimensions, *e.g.*, latency, accuracy, and transmission/resource cost. Moreover, energy savings in DL inference is also crucial for long-term running applications since most mobile AIoT devices are battery-powered [65], [66]. Also, it is desired to adapt the inference accuracy according to the resource availability and network condition for AIoT at runtime. We detail different levels of issues in the following part.

On-device DL Inference. Prior efforts explored several technologies to enable on-device DL inference, accelerate inference, and save memory occupation or energy. ***(i) resource-friendly algorithm level*** compresses DL models to reduce the resource demand without significantly compromising their accuracy. Standalone techniques include pruning [67], [68], [69], low-rank decomposition [70], lightweight architecture replacement [8], [12], [71], and parameter/activation quantization [72], [73]. Some research [74] also automatically combines diverse compression techniques to achieve better performance-resource tradeoffs. Although significant progress has been made in this field, compressed models typically yield accuracy degradation. ***(ii) model-adaptive system scheduling level*** spans multiple fine-grained levels, *i.e.*, computational graph [75]–[77], memory scheduling [12], [78], hardware instruction [79], [80], compiler front-end/back-end [76], [77], [81], and engine [12]. For example, existing DL frameworks, *e.g.*, Tensorflow [82], Pytorch [83], and TVM [9], provide support in computation graph and operator optimization. IOS [75] extensively studies the inter-operator parallelism to accelerate inference. Miao *et al.* [78] proposed dynamically swapping data between MCU's micro-SRAM and external flash to save SRAM. The suitable underlying scheduling can further improve resource availability than the algorithm-level compression models. However, most existing techniques are manually designed. ***(iii) intra-device cross-level controller*** aims to adaptively select the above-mentioned cross-level optimization techniques according to the user-specified performance demands and the device-imposed resource budgets. For example, AdaDeep [74] is an automated DNN compression framework at the algorithm level that uses deep reinforcement learning to balance performance and resources. MCUNet [12] performs joint optimization across the algorithm and engine levels, adapting the optimization strategies according to memory constraints. However, the combination criteria of cross-level techniques from a broader space remains a black box. ***(iv) inter-device cross-level controller*** will scale up the system from the on-device to distributed scheme once the large computing/memory resources required by executing computation-intensive models locally are unavailable.

Distributed DL Inference. Deploying different parts of DL models on multiple AIoT devices can harness the collective computational power of these devices, thereby decreasing local resource demands and enhancing inference efficiency. ***(i) resource-friendly algorithm level*** involves DL model partition [84], offloading [85], and performance tradeoff [85], [86]. According to the operator dependency of DL models and the resource availability of edge devices, various parts of DL models can be distributed to multiple devices for either sequential or parallel processing, resulting in different performance tradeoffs. For example, [86] jointly carries out the model partition and offloading to improve accuracy, energy consumption, and latency. ***(ii) model-adaptive system scheduling level*** includes computation graph partition [87], [88], distributed operator fusion [89], [90], separately data reuse and memory allocation. For example, Modnn [87] significantly speeds up DL inference by introducing execution parallelism among multiple devices [88]. Zhang *et al.* [91] proposes jointly optimizing heterogeneous chips' computing frequency, power, and memory to achieve the optimal allocation strategy on distributed devices. This area is relatively less explored. ***(iii) inter-device cross-level controller*** has a similar cross-level technique spectrum as the on-device inference scheme. And the fundamental difference lies in the fact that the underlying

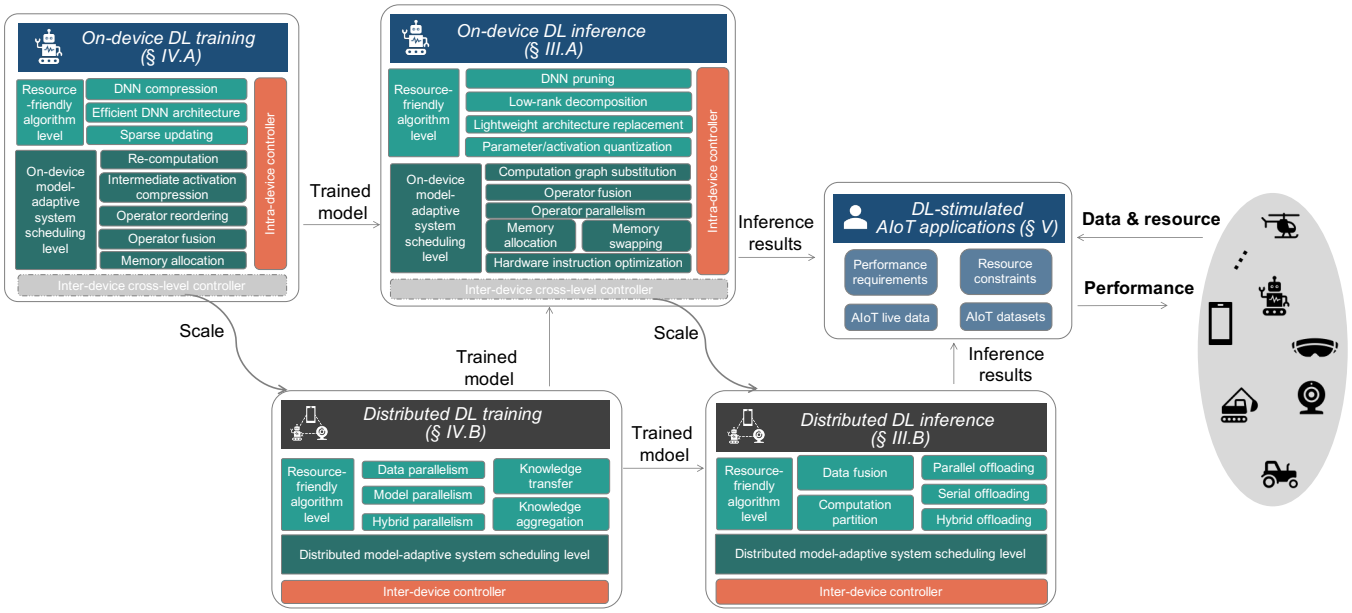


Fig. 6: Landscape of the resource-efficient AIoT system according to the proposed technique taxonomy.

operator and resource scheduling for distributed schemes must be *optimized separately and verified globally*. This is because different parts of the model deployed on multiple devices have separate memory pools and can not reuse data, necessitating separate optimization at diverse devices. Meanwhile, global evaluation is required for overall performance, such as the total latency of distributed execution and transmission. In addition, the controller selects the most suitable devices within the closely connected and resource-constrained edge. It involves the performance profiler [92], adaptive inference serialization or parallelism [93], and autonomatic optimizer [94].

2) Cross-level Optimization for DL Training Tasks: There are many demands for DL training on resource-scarce AIoT devices. For instance, we may need to update pre-trained DL models locally or nearby when the live sensing data drift to the original training data and an Internet connection to the cloud is unavailable. Other requirements for DL training on AIoT devices are also widespread, such as updating models to adapt to new applications. These requirements can be fulfilled using techniques like transfer learning [95] [96] [97] [98], domain adaptation [99] [100] [101] [102], continuous learning [103] [104] [105], and personalized federated learning [106] [107]. Besides, DL model fine-tuning is necessary after adaptive compression, which has been demonstrated in various practical scenarios [108] [109] [110] [111].

Challenges. It is intractable to realize low-cost DL training on AIoT devices. The reasons are three-fold: *i) resource constraint*. The bottleneck of embedded resources in AIoT devices is the memory access bandwidth [112]. While DL training needs *batched memory* chunks grouping multiple data samples for feature learning. Besides, the computation efficiency will be low if the memory for sufficient batch size cannot be secured. Because computations are highly sensitive to memory access schemes, *e.g.*, Cache hit rate [113]; *ii) irregular activation lifecycle*. The DL training phase involves forward propagation and backpropagation to update the model weights iteratively. Intermediate activations pose high memory demands, produced during the forward pass and reused during the backward pass [114]. In the case of DL inference using only forward propagation, resources occupied by activations can be directly released. However, during DL training involving both forward and backpropagation, activations must be retained throughout the process. Model structures, such as control flow and branching, affect the lifecycle of activations during backpropagation, which is less regular. Therefore, it is difficult to determine when data will be accessed for the last time and when it is safe to release resources. *(iii) multiple iterations.* Unlike DL inference's "one-time" property, DL training requires optimization across multiple iterations. Therefore, even small instabilities can be amplified over hundreds of iterations, potentially leading to the crash of DL training [38]. Additionally, current cloud-based DL training optimization techniques are not suitable for resource-scare AIoT devices.

On-device DL Training. Given these challenges, we summarize the enabling techniques in § IV-A that ensure sufficient resource supply and guarantee performance across different system levels. ***(i) resource-friendly algorithm level*** aims to reduce resource demands, especially memory usage, through model or training simplification. Techniques include model quantization [115], model compression [115]–[117], sparse updating [118], [119], *etc.* For example, TinyTL [112] presents the element-wise convolution decomposition to reduce memory, not parameters, for efficient on-device DL training. ***(ii) model-adaptive system scheduling level*** mainly optimizes three objects, *i.e.*, *intermediate activation*, *computation graph*, and *memory schedule*. Precisely, to trim down the *intermediate activation tensor* after the forward and before the backward pass, researchers present the recomputation [120], [121] and activation compression [122] techniques. They discard or compress the intermediate activation tensors to reduce the peak memory during DL training. Optimization techniques at the *computation graph* level include operator reordering [123] and

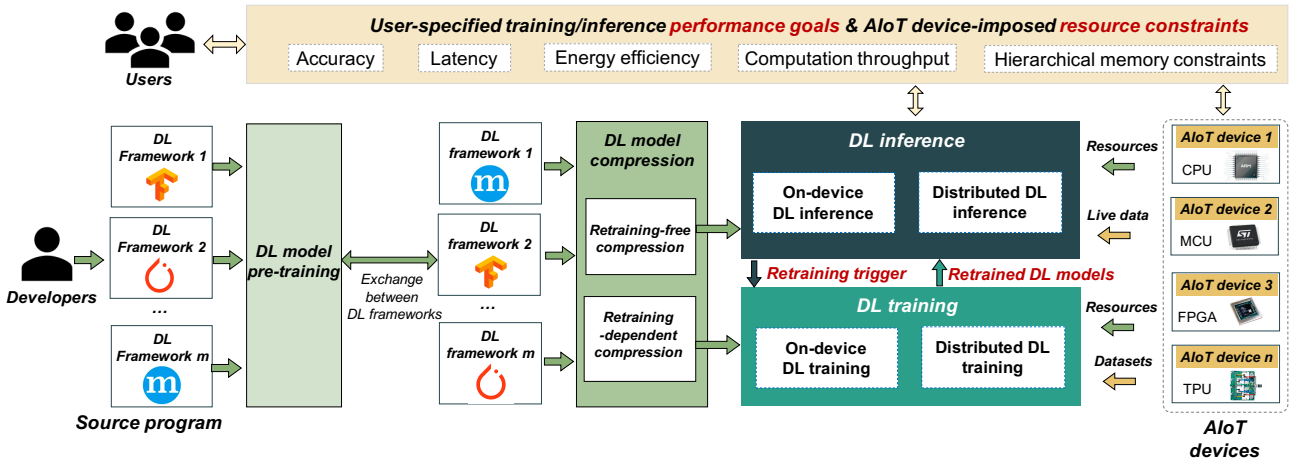


Fig. 7: Workflow of the AIoT system software for resource-efficient DL training and inference tasks on AIoT devices.

operator fusion [124], [125]. Rearranging or fusing operators in the computation graph can reduce memory usage and access delay. As for the *resource scheduling*, prior efforts mainly operate on memory, which is the lowest level optimization closest to hardware, including memory allocation [114] and memory swapping [39], [126]. For example, MoDNN temporarily swaps intermediate activation from graphics processing unit (GPU) memory to host memory to solve the problem of insufficient training memory and thereby realizes the optimal compromise between memory footprint and training speed [126]. ***(iii) intra-device cross-level controller*** jointly control multiple techniques across the above levels to achieve the best tradeoff between multiple conflicting performance goals for dynamic AIoT context. For example, adaptive precision training in [127] dynamically allocates model precision to balance training energy cost, memory usage, and accuracy.

Distributed DL Training. To coordinate data fusion and resource aggregation to optimize DL training efficacy and efficiency on distributed devices. We introduce cross-level enabling techniques for distributed training in § IV-B. In particular, ***(i) resource-friendly algorithm level*** optimizes the distributed training algorithm (*e.g.*, pipeline algorithm [128] and federated learning [129]) and changes the DL model/data partition strategy, which can significantly improve the distributed system's computing efficiency. ***(ii) model-adaptive system scheduling level***, like the on-device training, mainly optimize operator and memory access for training speedups and resource usage reduction, such as memory reallocation [130] and layer swapping [131] *etc.* For example, Zico [132] monitors the memory usage of each DL training task and reclaims the memory that is no longer needed, making it globally sharable in the system. ***(iii) inter-device cross-level controller*** considers all cross-level factors like the on-device DL training scheme. In addition, it considers the communication conditions, such as time-varying network throughput, to control the distributed system loop jointly. And it schedules the cross-level techniques separately and evaluates them globally. Specifically, it selects available devices to minimize overall training delay, ensure accuracy, and improve resource efficiency [133]. To address issues such as asynchronous processing and waiting times resulting from resource-heterogeneous AIoT devices, the inter-device controller should monitor their heterogeneity in advance and select suitable devices for collaboration.

D. Workflow Overview

Figure 7 showcases the resource-efficient AIoT system workflow and relationships of the system blocks for DL training and inference tasks. The system takes user-provided inputs, such as DL source programs, and aims to achieve user-specified performance goals while satisfying the resource constraints imposed by the AIoT devices. Specifically, the *user/developer* specifies the *DL source program* using various DL frameworks (*e.g.*, TensorFlow, Pytorch, Mindspore, *etc.*) and conducts model training using accumulated AIoT dataset. After DL pre-training, the model structure files are distributed to heterogeneous AIoT devices to analyze live data and provide intelligent services based on the pre-trained model. To be compatible with different DL frameworks in various AIoT devices, we can convert them to a unified format and exchange them (*e.g.*, using ONNX [134]). In the *DL inference phase*, we can select and combine the most suitable DNN compression techniques from the *model compression algorithm pools* to reduce the model complexity and resource demands. Most model compression techniques need to return to the training stage for several rounds of retraining to fine-tune model parameters to ensure accuracy [135]. And some recent efforts also realize the retraining-free model compression techniques, *e.g.*, through ensemble training of super-nets [136].

The resource-efficient *DL inference* includes on-device (§ III-A) and distributed (§ III-B) schemes. Particularly, it includes the runtime compilation front-end optimization (target platform-independent), the compilation back-end, and hardware instruction optimization (target platform-dependent). Both the compiler front-end and the back-end belong to the model-adaptive system scheduling level mentioned in § II-B. They convert the DL models designed at the algorithm level into intermediate representations, *i.e.*, computation graph, for further optimization. Compiler front-end optimization focuses on platform-independent optimization, such

as constant folding [137] [138] and common subexpression optimization [139]. And compiler back-end optimization focuses on platform-dependent optimization, such as operator fusion [140] [124], and memory allocation [141] [114].

When the accuracy of the DL model drops below a certain threshold due to changes in application scenarios, data, performance requirements, *etc.*, the *DL training* block is triggered to retrain and update the model. Whether the DL model is re-trained locally on a single AIoT device or on multiple locally-connected yet resource-constrained edge devices depends on how well the supply of device resources (*e.g.*, memory) matches the computing requirements for training and the desired training speed. Once the inter-device controller selects the training scheme, we can proceed to the on-device DL training optimization block (see § IV-A) or the distributed DL training block (see § IV-B). As a separate note, in resource-efficient AIoT system, the compiler optimization is cross-device [82] [9] on heterogeneous and distributed AIoT devices, *e.g.*, from GPU-based edge servers to MCUs, to support intelligent inference/training tasks. The inter-/intra-device controllers adaptively control the cross-level optimization strategies according to context information.

E. AIoT Performance Metrics

The resource-efficient AIoT system in both DL training and inference tasks needs to optimize the user-specified performance goals (*i.e.*, accuracy, latency, energy efficiency, computation throughput) and satisfy device-imposed resource constraints (*i.e.*, hierarchical memory, processor, battery). We listed the related metrics below:

1) Accuracy. The DL model should be accurate enough to guarantee a high-quality AIoT task. The model weights at different scales are well-trained to represent the generic information of recognition objects [142].

2) Memory. The parameters and activations of DL models should be appropriately sized to fit into the memory units of AIoT devices. We can directly calculate the memory needed to run a DL model using the total number of bits associated with weights and activations. And we should optimize how the operations access the data fetched from different memory hierarchies (*e.g.*, dynamic random access memory (DRAM), static random access memory (SRAM)) and how the computation is executed for latency or energy efficiency optimization [8].

- *Memory budgets*. The memory budget is a tough constraint; it decides whether a specific AIoT device can perform the DL inference or training tasks.
- *SRAM utilization*. Improving SRAM utilization and reducing DRAM transmission times can improve computing efficiency [143].
- *Cache/register hit rate* measures the percentage of times that the system is able to retrieve data from the cache in the central processing unit (CPU)/GPU [144] and register in MCU [145], instead of accessing it from the main memory. Higher cache/register hit rates mean that the system can access data more efficiently. We can use it to estimate the system efficiency in the presence of time-varying memory resources via run-time measurement [146].

3) Computational cost. It affects the AIoT system's latency and energy efficiency. We can model the computational cost of DL inference and training tasks as the total number of DL models' multiply-accumulate (MAC) operations.

4) Latency. The complexity of the DL model for inference and training should be controllable to meet diverse user demands on latency. The latency of DL inference/training tasks executed in AIoT devices strongly depends on the given device's architecture and memory hierarchy [147]. And we can refer to the latency predictor, such as nn-Meter [148], [149], for platform-aware latency estimation.

5) Energy efficiency. It is an important metric for battery-powered AIoT devices. Researchers usually formulate it offline and estimate it online since it is prohibitive to directly connect to energy monitors for measurement when the device is in service. The estimation methods include two types:

- *Estimation function*. The energy consumption of DL inference includes computation cost and memory access cost. The former can be formulated as the total energy cost of the total MACs, *i.e.*,, $E_c = \epsilon_1 C$, where ϵ_1 and C denote the energy cost per MAC operation and the total number of MACs, respectively. The latter depends on the storage scheme when executing DL models on the user-given embedded device. And the energy cost of fetching intermediate activations, *i.e.*, memory access, dominates in the DL inference phase.
- *Arithmetic intensity*. The hardware-aware metric, *e.g.*, arithmetic intensity, can proxy the degree of reuse of parameters and activations and the energy cost required for processing inputs [150], [151].

As a separate note, the widely used parameters number, MAC amount, or speedup ratio is not a good approximation for hardware efficiency (*e.g.*, energy cost, latency), which heavily depends on the underlying memory movement and bandwidth bound [8]. For example, Jha *et al.* [151] reported that although SqueezeNet [152] has $51.8\times$ fewer parameters than AlexNet, while it consumes 33% more energy due to its larger amount of activations and data movement. We identify that merely cutting down the parameter size may lead to an increase in activation size, which, in turn, increases the memory footprint, latency, and energy consumption [150].

The dynamic deployment context in continuously running AIoT applications often results in high levels of unpredictability and variability in terms of performance demands on the above metrics. This context includes factors such as agnostic AIoT sensing data, time-varying resource availability, dynamic join and exit of AIoT devices, and fluctuating inference/training request frequency triggered by real-world requirements. Thus, the resource-efficient AIoT system should continuously evolve to balance these metrics in a context-adaptive manner [8], [153].

III. Cross-level Optimization for DL inference

This section introduces existing efforts associated with the proposed challenges in cross-level AIoT systems and highlights how they have addressed some of them.

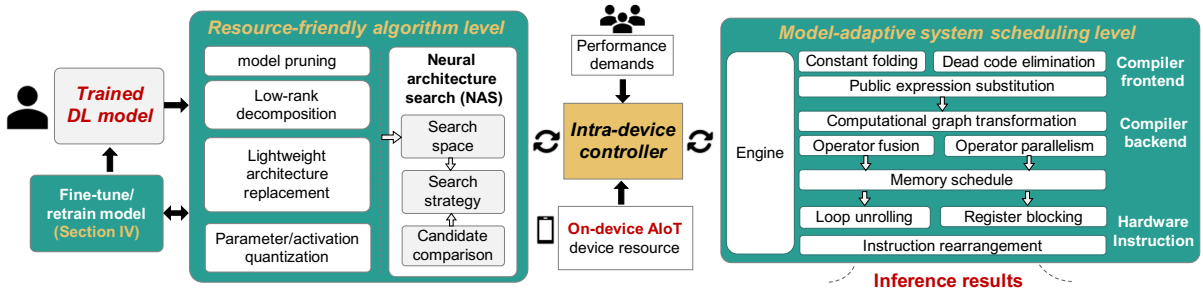


Fig. 8: System loop of the algorithm, system scheduling, and intra-device controller for on-device DL inference.

A. On-device DL Inference

An increasing trend in the field of AIoT is integrating DL-powered intelligence into local devices, allowing for analytics to be performed where the data is sensed. This approach offers advantages such as low transmission costs, network condition independence, and privacy preservation, as highlighted in [154], [155]. However, deploying DL models on resource-scarce local devices remains a challenging problem, as discussed in § II-C. To address this issue, cross-level optimization spans multiple levels (*e.g.*, model, computation graph, memory scheduling, hardware instruction, *etc.*) is essential. Additionally, context-aware controllers can further automate the on-device DL inference process. Figure 8 illustrates the on-device DL inference optimization pipeline.

1) Resource-friendly algorithm level: Algorithm-level optimization for on-device DL inference is extensively researched to minimize computation and memory requirements while preserving accuracy [154], [155] [156]–[161]. We briefly discuss some representative ones below.

a. Pruning. It reduces the model computation cost by removing redundant parameters [162], channels [69], or connections [163]. According to the grain size of pruning, it can be divided into synaptic pruning, neuron pruning, *etc.* Synaptic pruning cuts down unimportant connections between neurons, while neuron pruning removes neuron nodes directly. For example, Hu *et al.* [67] iteratively prunes neurons and uses the average percentage of zeros to find the unimportant activation. [68], [69] determine which channels must be pruned by minimizing the feature reconstruction error using greedy and Least Absolute Shrinkage and Selection Operator(*i.e.*, LASSO) regression optimizers, respectively.

b. Low-rank decomposition. Since model weight vectors are mostly distributed in low-rank subspaces, we can only use a few basis vectors to represent the convolution kernel for memory savings by combining dimensions or applying low-rank constraints [164], [165]. As shown in Figure 9,W_i is a large low-rank matrix which is decomposed into several small matrices such as $W_i^{(1)}, W_i^{(2)}, W_i^{(3)}, ..., W_i^{(k)}$.

Pavel Kaloshin [70] decomposed the tensor as a sum of low-rank and sparse components, approximating the convolution weights. The convolutional (conv) layers take the most execution time, and fully connected (fc) layers dominate storage costs. Lin *et al.* [166] jointly accelerates conv layers and compresses fc layers by utilizing low-rank decomposition to eliminate redundancy between conv kernels and fc matrices.

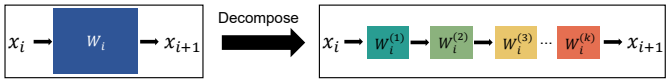


Fig. 9: Illustration of low-rank decomposition technique.

c. Lightweight architecture. Replacing large model blocks with lightweight architectures can adapt to resource-constrained AIoT devices. There are generally two categories, *i.e.*, block replacement [167] or neural architecture search (NAS) [168]. For example, Iandola *et al.* [152] replaced conv layers by Fire block, composing of a 1×1 conv layer and a conv layer with mixed 1×1 and 3×3 filters. Lin *et al.* [169] replaced conv by a micro multi-layer perceptron embedded with multiple small kernel conv (Mlpconv). To realize efficient DL inference on MicroController Unit (MCUs), with 2-3 orders of magnitude smaller memory than mobile phones, Lin *et al.* proposed MCUNet [12], Edgar *et al.* built μNAS [71] to specialize model architectures for MCUs automatically.

d. Parameter/activation quantization. Quantization [170], [171] refers to representing 32-bit floating-point model parameters with relatively low widths, including weight [172], activation value [173]. The model parameters can be unified with layer-wise low-bit-widths (*e.g.*, 16-bit, 8-bit, 2-bit, 1-bit, *etc.*) to reduce memory usage significantly, speed up computing, and reduce power cost. To adapt to the varying memory and computational limitations, Manuele *et al.* [72] modeled the DL inference graph by pure integer operation using mixed low-bit-width quantization. Under specific RAM and FLASH memory constraints in MCUs, Manuele *et al.* [73] use reinforcement learning to pick the best uniform quantization bitwidths for model weights and activations.

Discussion. Algorithm-level optimization techniques have shown great promise in reducing computation and memory requirements with slightly decreased accuracy. However, the degree of accuracy decrease is bounded by the runtime resource availability. While proposing new algorithms may lead to a slight improvement in performance-resource tradeoff,*e.g.*, latency, over existing techniques, their suitability to AIoT also depends on the system scheduling on the given hardware.

2) Model-adaptive system scheduling level: Joint optimization of system scheduling and upper-level algorithms has the potential to overcome performance bottlenecks. This level

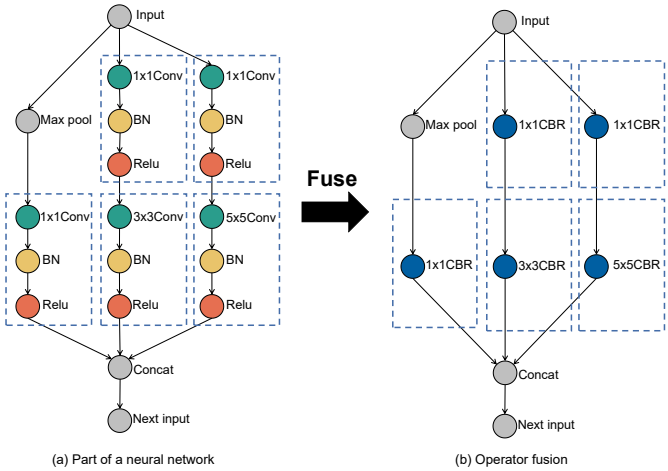


Fig. 10: Illustration of the operator fusion technique. (a) partial computation graph of GoogleNet, (b) longitudinally fuse *convolution, batchnorm* and *relu* into *CBR* operator.

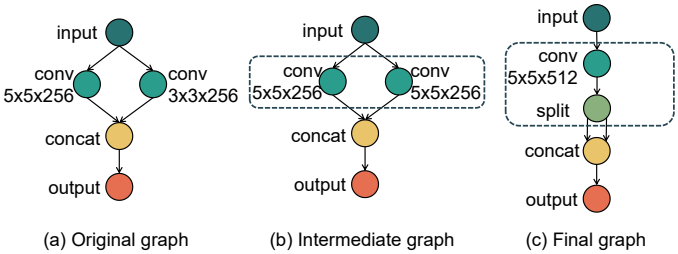


Fig. 11: Illustration of the computation graph substitution technique. (a) original computation graph includes *convolution* operators, (b) expanding smaller conv kernels, and (c) merging two conv operators into one.

aims to utilize hardware resources to their fullest capacity without compromising model accuracy. The system scheduling for DL inference mainly includes the compiler front-end (*i.e.*, device-independent) and compiler back-end (*i.e.*, device-dependent). Compiler front-end optimization aims to eliminate redundancy and simplify the computation of the intermediate representation (*i.e.*, computation graph) during compilation. It is device-independent and contains constant folding [174], dead code elimination [174], *etc.* And compiler back-end aims to use hardware resources to execute DL inference tasks fully. It mainly focuses on computation graph-level optimization (*e.g.*, operator fusion [81], computation graph substitution [124], [175]), operator parallelism [75], [176], memory-level optimization (*e.g.*, memory allocation [177], [178], memory swapping [78], [179]), and hardware instruction optimization (*e.g.*, loop unrolling [180], register blocking [80]). We introduce some representative enabling techniques below.

a. Operator fusion. Despite the massive size of model parameters, the intermediate feature maps extracted from the input data can quickly become too large and consume significant amounts of memory. This is especially problematic because these intermediate feature maps are often used as inputs for multiple operators in the computation graph, leading to increased memory access and processing delays. One solution to this problem is to fuse adjacent operators in the computation graph into a new operator according to certain rules. Figure 10 illustrates an example in GoogleNet. The original operators include convolution, batchnorm, relu, max pool, and concat, as shown in Figure 10a. Then *convolution, batchnorm* and *relu* operators are fused into the *CBR* operator. They have the same computation results. However, the number of model layers in Figure 10b is decreased, the data channel is shortened, and the memory access frequency of the intermediate feature maps is reduced, so the inference speed is improved. Han *et al.* [181] expand the CBR operator fusion to TensorRT.

Existing DL frameworks such as TensorFlow Lite [26], TVM [9], MNN [182], and Pytorch-Mobile [28] have provided application programming interfaces (APIs) for operator fusion. However, most of them only provide fixed operator fusion patterns, and the operator fusion types are still insufficient to support diverse DL operators and connections. Niu *et al.* [77] proposed a universal fusion framework called DNNFusion. It divides operators into different types according to their input and output forms, develops operator fusion plans after comparing the performance of diverse fused operators, and conducts extra optimizations such as reducing redundancy during the fusion code generation. This approach based on general operator type greatly expands the operator fusion opportunity. Experimental results show that the operator fusion space is expanded by 8.8×, and the inference speed exceeds the advanced frameworks (*e.g.*, MNN [182], TVM [9], Pytorch [176], TensorFlow Lite [26]) by up to 9.3×. Another problem is that the operator fusion space and memory efficiency lack direct mapping, making it difficult to access optimal memory. Cai *et al.* [76] proposed an operator fusion framework, Optimus, based on directed acyclic graphs. It can be applied to several DL models running on accelerators. Experiments show that Optimus reduces inference memory access overhead by 17-75% and improves efficiency by 1.86-3.66×. Furthermore, automated operator fusion, instead of manually crafted fusion, can greatly enhance the performance of complicated or previously unseen operator chains.

b. Computation graph substitution. Computation graph substitution techniques replace the subgraph with another functionally equivalent subgraph to reduce the amount of computation and delay. For better understanding, Figure 11 shows an example. In the original graph (see Figure 11a), there are two *conv* operators that have 256 kernels with 3×3 size and 256 kernels with 5×5 size, respectively. We can first expand all 3×3 kernels to 5×5 (see Figure 11b), merge two 5×256 conv operators into one 5×512 conv operator, and then separate them using *split* operator before executing the *concat* operator (see Fig. 11c). Via computation graph substitution, we remove the computational-intensive conv operator. And the computational cost of the *split* operator is almost negligible.

Existing DL frameworks (*e.g.*, PyTorch [176], TensorFlow [82]) substitute computation graphs using greedy rules or manual methods, which, however, cannot guarantee the selection or combination bring rigorous improvements. Jia *et al.* [124] proposed an optimizer for graph substitution.

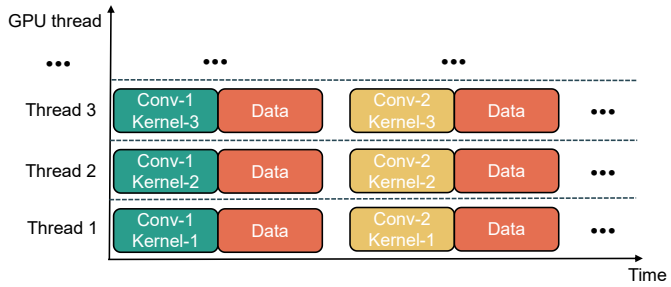


Fig. 12: Illustration of intra-operator parallelism technique. The conv operator kernels and data are divided into different groups and deployed on different threads to execute in parallel.

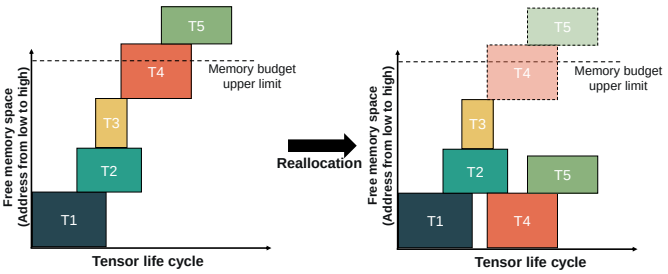
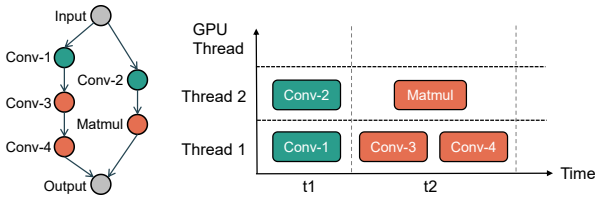


Fig. 14: Illustration of memory allocation technique. After reallocating the memory position of tensors, the memory peak is reduced without conflicting access to the tensor.



(a) Computation graph (b) Inter-operator parallelism

Fig. 13: Illustration of inter-operator parallelism technique. (a) the original computation graph, (b) two conv operators execute in parallel on different threads during the t_1 time period. During the t_2 time period, the *matmul* operator executes on thread 2, while the serial execution of two *conv* operators execute on thread 1.

They automatically use a cost-based search algorithm on the graph substitution space to find the optimal solution. Jia *et al.* [183] proposes an optimizer (*i.e.*, TASO) to substitute the computation graph automatically. TASO generates several candidates for a given list of operators and picks the most suitable substitutions. Experiments show that TASO outperforms existing DL frameworks by 2.8× and significantly reduces human labor. Fang *et al.* [175] formally defined the computation graph substitution problem (*i.e.*, OCGGS) and narrowed the search space to sample the best solution.

c. Operator parallelism. There are two kinds of operator parallelism techniques, *i.e.*, intra-operator and inter-operator parallelism. Mainstream AIoT platforms always equip with multi-core CPUs and multi-core GPUs. Considering the increasing speed gap of diverse processors (*e.g.*, CPU and GPU), separate methods are designed for the CPU and GPU to overcome the memory access bottleneck. For CPU devices, the cache hides delays in accessing memory to reduce the pressure on memory bandwidth. GPUs do not use or only use relatively small caches, mainly through the parallelism of threads, to hide the memory access delay. When some threads are stuck due to memory access, another part of the threads will continue to execute and will not let processing units idle.

Intra-operator parallelism. Existing DL frameworks (*e.g.*, TensorFlow [82], PyTorch [176]) can support intra-operator parallelism, *i.e.*, parallelizing arithmetic operations (*e.g.*, convolution) within a single operator. In the convolution operator, kernels that will be executed on the same thread are divided into one group, and then the corresponding data is also grouped. Then, different groups of conv kernels and data are deployed on diverse threads for parallel execution, as shown in Figure 12. However, as high-performance hardware evolves, intra-operator parallelism is no longer efficient enough.

Inter-operator parallelism. Inter-operator parallelism allows multiple operators to execute on different threads in parallel, as shown in Figure 13. Ding *et al.* [75] proposed an inter-operator scheduler(*i.e.*, IOS). IOS can search highly optimized parallel schemes using a dynamic programming algorithm. And this approach can be generalized to existing DL frameworks. Experimental results show that IOS increases the inference speed by $1.1\times \sim 1.5\times$.

d. Memory allocation DL model parameters and intermediate activations take up large memory resources during forward propagation as models become more complex. The default memory allocation schemes by the operating system (*i.e.*, OS) always result in memory fragmentations, which cannot be used for other tasks. To solve this problem, memory reallocation is necessary. During DL inference, input tensors, weights, and intermediate activations are all one-offs, we can release them from memory in time after use. Also, we can allocate the same memory to different tensors that do not coincide with the usage time. As shown in Figure 14, T1 $\sim$ T5 represent a set of tensors. If we allocate memory for each tensor in order, it will easily reach the memory limit, like tensors T4 and T5. And since the lifetime of tensor T4 is completely disjoint with T1, they can be allocated in the same memory block. Similarly, T5 and T2 can also share memory.

Sekiyama *et al.* [184] proposed a profiler-guided memory allocation method. During propagation, they collected information about requested memory blocks and then allocated memory using a heuristic algorithm to reduce peak memory footprint. By experimenting on advanced DL models, they reduced memory footprint by nearly 50% and improved inference speed by 4×. To consider the layer diversity of computation and communication, Wei *et al.* [177] designed a layer-wise memory allocation framework on Field Programmable Gate Array(*i.e.*, field-programmable gate array(FPGA)). They used the layer diversity and the non-overlapping lifespan information of memory buffers to schedule on-chip memory.

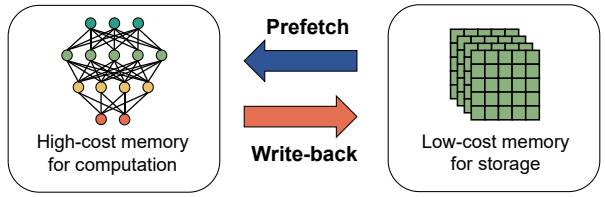
TABLE I: Summary of model-adaptive system scheduling-level enabling techniques for on-device DL inference.

Category			Technique highlight for improving	Device	Year	Ref.	Compiler frontend	Compiler backend
Model-adaptive system scheduling level	Computation graph level	Operator fusion	Circular fusion, operator classification, reduce redundancy, reduce computation latency	Mobile phone	2021	[77]	✓	
			Directed acyclic graphs, accurate memory cost model, reduce computation latency	Cloud server	2022	[76]		✓
			Candidate exploration, selection of fusion plans, code generation of local and distributed operations, reduce computation latency	MPU	2018	[81]	✓	
		Computation graph substitution	Relaxed graph substitution, backtracking search algorithm, flow-based graph split algorithm, reduce computation latency	Cloud server	2019	[124]		✓
			The first DL computation graph optimizer, automated theorem prover, cost-based backtracking search, reduce computation latency	Cloud server	2019	[183]		✓
			Pruning-based algorithm, sampling heuristic, reduce computation latency and memory usage	Cloud server	2020	[175]	✓	
		Operator parallelism	Intra-operator parallelism, reduce computation latency	Cloud server	2016	[82]		✓
			Intra-operator parallelism, reduce computation latency	Cloud server	2019	[176]		✓
			Inter-operator parallelism, inter-operator scheduler, novel dynamic programming algorithm, reduce computation latency	Cloud server	2021	[75]		✓
	Resource scheduling level	Memory allocation	Novel profile-guided memory optimization, heuristic algorithm, reduce computation latency and memory usage	Cloud server	2018	[184]		✓
			Memory allocation algorithm, memory bound layers, reduce computation latency and memory usage	FPGA	2019	[177]		✓
			Loop-orderbased memory allocation, fast auto-scheduling methodology, reduce computation latency and memory usage	Cloud server	2021	[178]		✓
		Memory swapping	The first memory swapping on MCU, swap data block between SRAM and FLASH or SD card, reduce memory usage	MCU	2021	[78]		✓
			Joint optimization along 3 dimensions, custom-designed genetic algorithm, reduce computation latency and memory usage	Cloud server	2020	[185]		✓
			Swap model parameters from the external storage into DRAM, task bounded with subnet, reduce computation latency	Cloud server	2022	[179]		✓
	Hardware instruction optimization	Loop unrolling	A generalized loop-unrolling method for any type of loop construct, reduce computation latency	Cloud server	1999	[79]		✓
			A semi-automatic and compile-time approach for identifying the optimal unroll factors, reduce computation latency	Cloud server	2010	[180]		✓
		Register blocking	A performance model to set the appropriate register block size, reduce computation latency	MPU	2001	[80]		✓
		Instruction reordering	A flexible multi-criteria instruction reordering heuristic that can be adapted across architectures, reduce computation latency	Cloud server	2018	[186]		✓

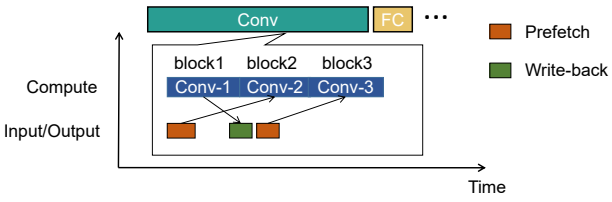
The hit rate on the hardware accelerator and the memory allocation policy mapping can also affect its performance. To search for the best map fastly, many works redesigned the search space, *e.g.*, state-of-the-art [187]–[190]. However, the efficiency in these DL frameworks is still slow due to exhaustive searches. And it does not consider the user-defined or random-sampled constraints, thereby cannot guarantee the global optimum. Also, they cannot deterministically assess the optimality because predicting the needed CPU time and peak memory in advance is prohibitive. To address this problem, Symons *et al.* [178] allocated memory based on the loop order. It takes advantage of DL models' nested "FOR" loop sequence and assigns them to the most appropriate memory hierarchy.

e. Memory swapping. Memory swapping [185], [191] refers to the exchange of tensors or data chunks between the high-cost memory and the low-cost one during computation. For example, when the device's memory supply cannot meet the tensors' demands, we can swap out partial tensors to free up space and serve current operations. The focus of memory swapping in the inference phase differs from that in the training phase. The training phase focuses more on the reuse of tensors during backpropagation. While the inference mainly focuses on forward propagation, *e.g.*, prefetching of tensors and the write-back after the computation is completed on memory-scarce AIoT devices, as shown in Figure 15a. However, memory swapping brings transmission delay. To solve this problem, some works propose to cover the transmission delay with the computation delay so that the transmission delay does not affect the overall delay. When the device resources are extremely limited, the model can be divided into several blocks for execution. For example, as shown in Figure 15b, when block 1 is executed, the parameters required by block 2 are prefetched, and the result is written back to the low-cost memory after block 1 is executed.

Miao *et al.* [78] proposed a system solution for deploying DL models on MCUs. It dynamically swapped model blocks between the SRAM and flash of MCU. This method trades time for space, thus not affecting accuracy. Besides, swapping



(a) Memory swapping process.



(b) Memory swapping delay.

Fig. 15: Illustration of memory swapping techniques for on-device DL inference.

tensors between GPU and CPU is also efficient because the GPU is fast with small memory. In contrast, the CPU has relatively large memory to store temporary tensors. And this method becomes more promising with the development of current GPUs. They can realize cross-communication and computation based on generous communication bandwidth. Huang *et al.* [185] proposed a universal swapping system called SwapAdvisor. It establishes search space with memory allocation and operator scheduling techniques and uses a genetic algorithm to determine exactly when and which tensors to swap before execution. SwapAdvisor breaks through the GPU memory limit by 12× and increases the inference speed by 4×. Ji *et al.* [179] proposed task-aware swapping(*i.e.*, TAS) for object detection tasks on IoT devices. Since the same type of task involves the same subnetwork, TAS swapped the model parameters of the corresponding subnetwork from external memory to dynamic random access memory(*i.e.*, DRAM) in time, according to different task types. TAS reduced the DRAM memory by 34.6% while maintaining accuracy.

f. Hardware instruction optimization. DL inference optimization on AIoT devices also includes the following hardware instruction optimization techniques:

Loop unrolling. It is a widely known code conversion method to improve program execution performance. The unrolled loop typically executes fewer instructions than the original one. As shown in Figure 16, the assembly loop code on the right is unrolled, and the calculation is reduced from 404 to 229 times. Thus loop unrolling can speed up calculations. Huang *et al.* [79] proposes a generic loop unrolling approach for diverse loop structures (*e.g.*, FOR, WHILE, DO-WHILE). The loop unrolling support in the GPU compiler is limited. Giridhar [180] developed a semi-automatic compiler to identify the optimal unrolling factor based on compile-time characteristics and the effect of loop unrolling on the program.

Register blocking. It rationally blocks registers to reduce idleness and increase register multiplexing. Based on matrix-independent device features, Sparsity [80] proposes a performance model to set the appropriate register block size, hence optimizing the sparse matrix computation speed.

Instruction reordering. It scrambles the instructions of different execution units to improve the utilization rate of the pipeline. Rawat *et al.* [186] proposed a flexible multi-criteria heuristic based on instruction reordering, which can be adapted across architectures.This approach alleviates register pressure while properly controlling the degree of parallelism at the instruction level.

The compiler or CPU/GPU/TPU processor can reorder instructions to optimize the execution performance of the program. For example, instructions with high delay are advanced, and data dependence before and after instructions is reduced. From the source program to the final running instructions, there are two stages of reordering:

Compiler reordering. During compilation, without affecting the result of the program, the compiler reorders instructions based on context analysis to reduce the interaction between CPU and memory. After rearranging, the CPU can read data from registers or cache rows as much as possible.

Processor reordering. It includes *parallel instruction set reordering* and *memory system reordering*. First, in the *parallel instruction set reordering*, modern processors use Instruction-Level Parallelism (ILP) to execute multiple instructions. The processor changes the order in which a statement corresponds to a device's instruction. As shown in Figure 17, the CPU hopes to execute the *instruction 1* and *instruction 2* in parallel. However, both them assign value to the same register *eax*, so the value saved in the final register *eax* is not the result of two addition computations. As a result, the value saved in register *ebx* is incorrect. Therefore, *instruction 1*, *instruction 2*, and *instruction 3* are executed serially. At the same time, the CPU needs to select one of the subsequent instructions (*i.e.*, *instruction 4*) to execute with *instruction 1* in parallel. With the reordered instruction set, parallel execution can be more efficient. Second, as for the *memory system reordering*, since the processor uses cache and read/write buffers, loading and storing operations is performed out of order. Therefore, memory system reordering should be well-designed.

3) Intra-device cross-level controller: The controller is required upon the above optimization techniques to automatically adapt to diverse performance requirements of AIoT applications and resource budgets of AIoT devices. Liu *et al.* proposed AdaDeep [74], which leverages the deep reinforcement learning-based optimizer to automatically select the most appropriate combination of compression techniques and hyperparameters for a given DL model in a hierarchical manner. Yang *et al.* [192] proposed an energy-aware CNN pruning algorithm, which automatically guides the pruning process by using the energy estimation of DL model. Edgar *et al.* [71] automatically design suitable DL models for MCUs, achieving high accuracy while achieving low memory usage and latency. MCUNet [12] is an example of cross-level system optimization, which can drive better optimization strategies. They jointly optimize the DL algorithms by TinyNAS and the memory scheduling by TinyEngine to reduce memory usage. TinyNAS automatically optimizes the search space

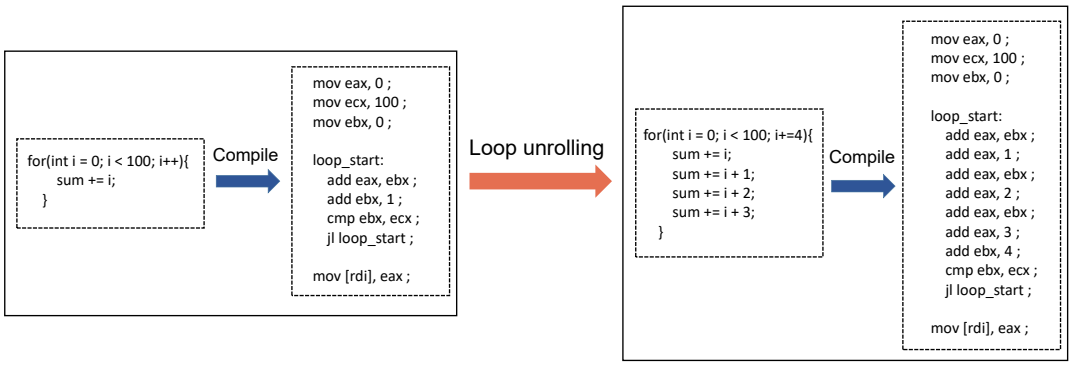


Fig. 16: An example of loop unrolling technique.

TABLE II: Summary of related intra-device controllers for on-device DL inference.

Category	Context awareness	Controller	Cross-level	Optimizated performance	Year	Ref.
Controller	Latency, memory	DQN, DDPG	Algorithm level	Accuracy, energy consumption	2020	[74]
	Accuracy	/	Algorithm level	Energy consumption	2017	[192]
	Peak memory usage, model size, latency	Multiobjective constrained NAS algorithm	Algorithm level	Accuracy, peak memory usage, model size, latency	2021	[71]
	Latency, energy, memory	Two-stage NAS for tiny memory constraints	Algorithm level & compiler level	Latency, memory	2020	[12]

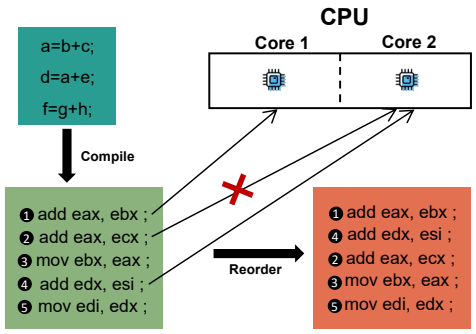


Fig. 17: Illustration of parallel instruction set reordering technique. The digits $1 \sim 5$ represent the instruction ID, not the actual execution order.

to fit the tiny resource constraints in MCUs. TinyEngine improves the existing inference library with code generator-based compilation methods to eliminate memory overhead. MCUNet has improved inference speed by 3.4× and reduced the peak memory footprint on SRAM by 4.1 ×.

B. Distributed DL Inference

In addition to on-device optimizing to reduce the resource demands of DL models for local adaptation, distributed DL inference aims to aggregate more resources from multiple devices within the networked AIoT systems to improve inference efficiency. This is achieved by partitioning the intensive computations of DL inference tasks and offloading diver portions of them to multiple devices. Distributed DL inference is particularly beneficial given the increasingly complex structure of modern DL models, which often require memory and computing resources far beyond the limits of a single AIoT device. For example, MCUs typically have only 256kb of memory, while ResNet, a widely-used model, requires 7.2MB for parameter storage.

Given the challenges mentioned in II-B, we divide distributed DL inference optimization into the resource-friendly algorithm level, model-adaptive system scheduling level, and inter-device controller, as shown in Figure 18. The algorithm and system scheduling levels focus on improving the resource efficiency of given heterogeneous hardware from different aspects. The inter-device controller automatically selects devices and cross-level techniques according to dynamic AIoT context.

1) Resource-friendly algorithm level: It mainly specifies the model partition and offloading schemes for satisfying distributed inference performance demands and resource budgets. We classify them as *layer-wise* and *operator-wise* categories. Specifically, the layer-wise scheme refers to partitioning and offloading the model according to model layers. And the operator-wise scheme goes deep inside layers, *e.g.*, optimizes the operator itself or the connection between operators.

Layer-wise scheme. Several studies [84], [196]–[198] have put forward the layer-wise distributed DL inference. Yun *et al.* [84] specialized the lightweight models by knowledge distillation and selected model partition points to minimize inference delay and satisfy the resource limitations of end devices (*e.g.*, Raspberry Pi 3B). Wu *et al.* [85] expressed the data sampling rate and model offloading problem as a constrained Markov decision process and obtained a heuristic solution. He *et al.* [86] model the arrival process of DL inference tasks as Poisson distribution. And they established a multi-faceted evaluation method [199], [200] to profile the inference latency, accuracy, memory usage, *etc.* DeeperThings [90] established the joint optimization of model partition and device selection

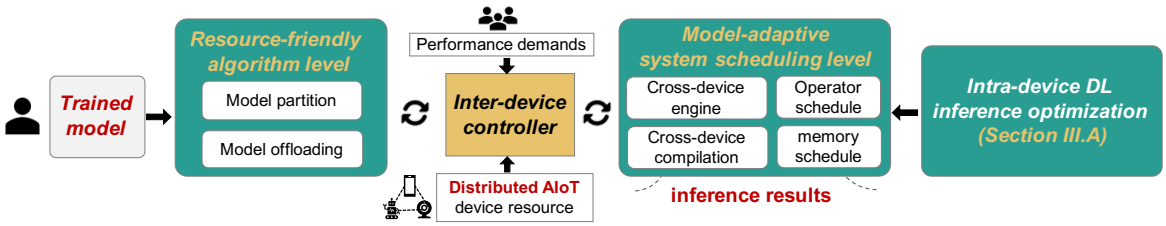
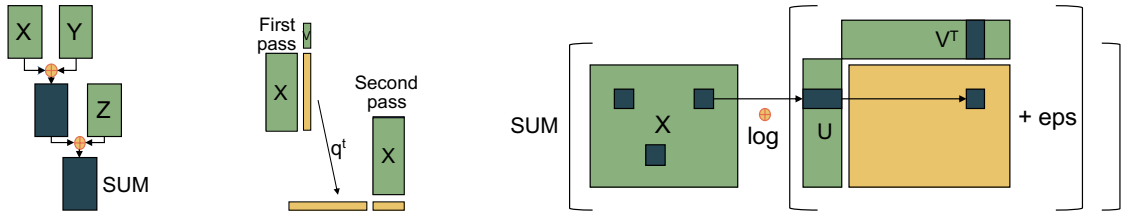


Fig. 18: System loop of the algorithm, system scheduling, and inter-device controller for distributed DL inference.



(a) Intermediates (b) Single-pass (c) Sparsity exploitation

Fig. 19: Illustration of code fusion techniques. (a) Code fusion can eliminate the intermediate in the computing, $sum(X \oplus Y \oplus Z)$; (b) code fusion can eliminate unnecessary scans of inputs, $X^T(Xv) \rightarrow ((Xv)^T X)^T$; (c) code fusion allows sparsity exploitation across chains of operations, $sum(X \oplus \log(UV^T + eps))$.

TABLE III: Summary of cross-level optimization techniques for distributed DL inference.

Focus level	Technique highlight for improving resource efficiency	Offloading	Year	Ref.
DL model	Multi-dimensional resource management, deep reinforcement learning	Serial	2021	[91]
	Constrain Markov decision process, Lyapunov optimization	Serial	2020	[85]
	Single batch inference, use several new model parallel methods	Parallel	2020	[93]
Operator	Operator fusion, distributed code generation	Hybird	2018	[81]
	Scalable convolution layer fusion, improve data reuse	Parallel	2018	[89]
	Partition computing layer, integer linear programming	Parallel	2021	[90]
	Convolution layer fusion and tiling, memory usage predictor	Hybird	2021	[193]
	Partition the full connection layer, cover all layers	Parallel	2019	[194]
	Vertical partition, weight pruning technique	Parallel	2022	[195]
Computation graph	Memory-constrained, joint optimization, knowledge distillation	Serial	2022	[84]
	Delay-Sensitive, mixed integer nonlinear programming,mec server	Hybird	2020	[86]
	Distributed model computing system, dynamic partition	Parallel	2020	[92]
	Reduce non-parallel data transfer time, convolution segmentation	Hybird	2017	[87]
Inter-device controller	Supports customized flexible fine-grained scheduling	Parallel	2021	[94]
	Greedy two-dimensional partition, structured models are tightly deployed	Hybird	2017	[88]

as a nonlinear programming problem. He *et al.* [86] designed a CRA algorithm based on Markov approximation to search the solution quickly, *e.g.*, 350 ms for a 10-device cluster.

Operator-wise scheme. Most studies focus on integrating and reallocating operators to reduce memory footprint. Specifically, merging more operators helps reduce the memory footprint of intermediate outputs and achieve better cross-operator sparsity development. For example, Boehe *et al.* [81] reduced the intermediate activation of the fusion of different operators and designed a cross-operator sparsity plan to improve computational efficiency. Stahl *et al.* [194] conducted research on layer operator fusion and reduced the data transmission time between multiple devices by combining feature and weight division with communication-aware layer fusion methods. Further, Farley *et al.* [193] design an independent fusion scheme for conv layer and fc layers, which reduces memory overhead through data reuse. However, these works lead to high synchronization overhead. To this end, Zhang *et al.* [94] presented an adaptive cooperative inference system that supports mainstream models (*e.g.*, ResNet, GoogleNet). And it provides a set of APIs to obtain the data location for enabling fine-grained scheduling and memory reclamation.

2) Model-adaptive system scheduling level: This level aims to optimize the input data reuse, intermediate data movement, and memory overhead (*e.g.*, memory fragmentation and recycle) in distributed DL inference [87]–[90], [201], [202]. It should be optimized separately at each device and verified globally cross-device. And how DL models offload to multiple AIoT devices affects the separate system scheduling technique selection and global performance verification. The existing

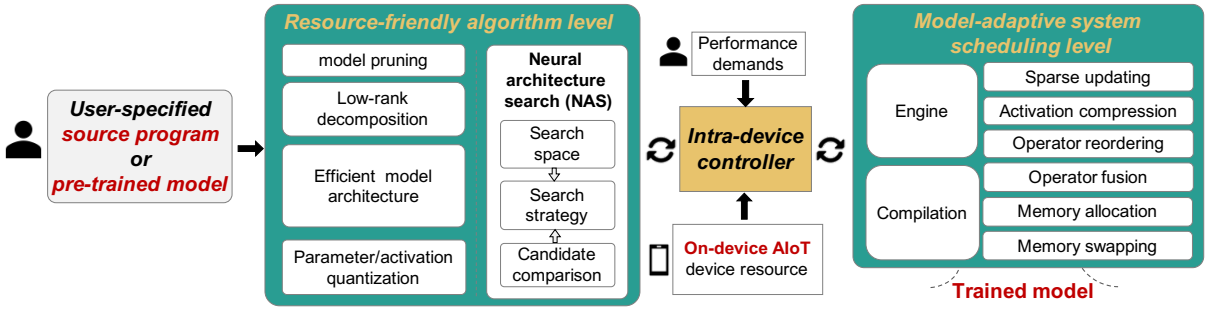


Fig. 20: System loop of the algorithm, system scheduling, and intra-device controller for on-device DL training.

DL model offloading schemes can be serial [84], [85], [91], parallel [89], [90], and hybrid [88], [193], [203]. For example, MoDNN [87] partitions the conv layer and distributes them to diverse AIoT devices for parallel computing. It partitions the input of the conv layer according to the matrix size and balanced unloading and sends them to different devices for collaborative inference. MeDNN [88] is an improvement of MoDNN, solving the problem of unbalanced model partition. It proposes a greedy 2D model segmentation algorithm to perform static load balancing according to the computing power of each device. Further to Mednn, Deepthing [89] proposed the improved solution. It proposed a scalable method to merge and partition the convolution layer by dividing the input matrix into different areas and unloading it to different devices for inference. It implemented a distributed job-stealing approach to realize dynamic workload allocation and computational efficiency balance, improving data reuse by 68% and reducing latency by $\geq$ 1.7 times. Another study [193] also explores the fusion and optimization of CNNs. Besides, it is difficult for existing operator fusion heuristics to develop distributed operator fusion schemes for complex models, *e.g.*, DAGs. Matthias *et al.* [81] proposed an optimization framework for systematic inference fusion schemes, Figure 19 shows three main ways of code fusion.

3) Inter-device cross-level controller: The context-aware controller can automatically adapt to varying contexts without re-designing systems, which is necessary for long-term running applications. Adjusting the distributed inference configurations for dynamic demands and heterogeneous devices is one of the recent research focuses [93], [94], [182], [204]. Haddi *et al.* [93] integrates multiple existing parallelism inference technologies into an automated framework. Zhang *et al.* [94] proposed Deepslicing, an adaptive control system integrating multipliers and deep reinforcement learning. It also exposes a set of APIs to users for adaptation. However, the controller across several AIoT system levels, especially the underlying system scheduling level, is still lacking.

To be compatible with heterogeneous AIoT devices and boost the inference efficiency, prior efforts also present the inter-device schedule frameworks, such as [92], [205]–[207], adapting to heterogeneous AIoT platforms/clusters. For example, Zeng *et al.* [92] presents Coedge. It involves a distributed DL inference framework and a fast approximate solution to determine the optimal platform scheduling strategies. Zhang *et al.* [91] considers the embedded chips' memory limits, computing frequency, and battery and transforms the hybrid optimization problem into a Markov decision process. As a result, it reduces inference delay and pushes the average accuracy limit caused by pre-determined resource allocation.

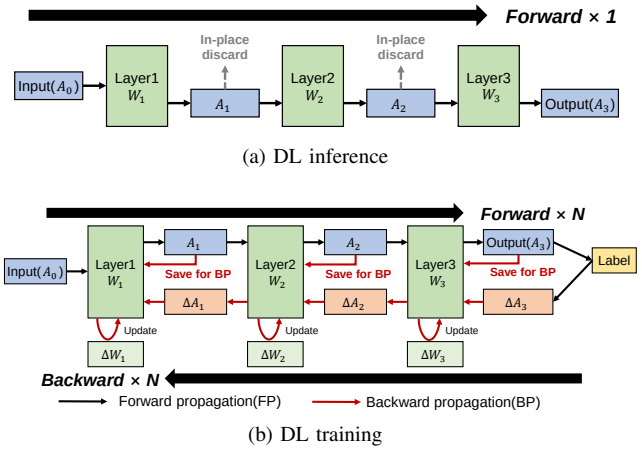
Discussion. Table I summarizes the standalone system scheduling techniques. And Table III illustrates the enabling techniques for distributed DL inference optimization across diverse levels. The performance of different levels of optimization techniques on the same DL model varies. And even within the same level of optimization techniques, their performance also differs. Existing DL frameworks for AIoT devices already support the techniques mentioned in this table. However, the criterion for their cross-level combination in the context of AIoT applications need more exploration. Moreover, combining diverse techniques across these levels with an adaptive and automatic controller is still lacking.

IV. Cross-level Optimization for DL Training

DL training adopts *batched memory* chunks grouping multiple data samples. And the memory usage increases proportionately to the batch size. Specifically, the computation efficiency will be low if not secure sufficient batch size. Larger batch sizes can bring more accurate distribution statistics for operators like BatchNorm [208] to speed up the training convergence and increase the accuracy.

We first **differentiate the specificities of DL training** from DL inference in terms of memory and computation demands, as shown in Figure 21. *(i)* DL training requires more computation than inference. More memory access during the training process also brings more memory access delay. For example, the bottleneck of GPU computing power for the GPU devices always lies in the memory access bandwidth and the upgrade of successive generations of GPU focusing on memory bandwidth proves this point [112].

(ii) DL training requires more memory space than inference. According to the chain derivative rule of backpropagation, calculating the gradient and derivative of the weights in the i^{th} layer requires using the derivative of the $i+1^{th}$ layer and the input of this layer. Therefore, the *intermediate activations* A_1, A_2 produced during forward propagation need to be saved till backpropagation calculating the gradients ΔA, ΔB and updating the weights during backpropagation. In contrast, A_1, A_2 in model inference process do not need to be preserved.



(a) DL inference

(b) DL training

Fig. 21: Comparison illustration of DL training and inference. (a) Inference only requires once forward propagation(FP), and intermediate activation tensor Ai can be discarded to reduce memory usage. (b) In training, tensor Ai needs to be saved for back propagation after the forward propagation.

They can be released right after they have been used, which brings a bigger memory requirement to the training process.

(iii) DL training needs N rounds of loop iteration, while inference needs only one round. For algorithm level (*e.g.*, model parameter/activation quantization), if not carefully designed, the tiny instabilities generated will be amplified in thousands of iterations and even leads to training crash [38]. Compared to the "one-time" property of the model inference process, DL training needs to consider optimization across *multiple iterations*, which also challenges system optimization.

A. On-device DL Training

It is non-trivial to optimize three key performance metrics, *i.e.*, *latency*, *memory*, and *accuracy*, simultaneously for on-device DL training. Given challenges towards optimizing memory usage, latency, and accuracy simultaneously (see § II-C), we summarize the on-device DL training optimization techniques into diverse system levels as described in § II-B, *i.e.*, the resource-friendly algorithm level, model-adaptive system scheduling level, and inter-device controller. Figure 20 shows their relationships in the system loop.

1) Resource-friendly algorithm level: We first briefly introduce the algorithm-level techniques, *i.e.*, compressing DL model structure [116] [209], reducing parameter/activation bit width [115] [210], and sparse updating [118] [119].

a. Parameter/activation quantization. DL model quantization during training is more complicated than inference since it brings instability to training [211] [212] [213]. Deng *et al.* [115] conducted the first exploration of model quantitation in DL training. They implemented reduced-precision memory access of parameters and saved significant memory bandwidth using an approximator. Subsequently, Zhou *et al.* [210] train DL models with low-bit width weights, activations, and gradients on diverse devices, *e.g.*, CPU, GPU, application specific integrated circuit(ASIC), and FPGA, to speed up training. Besides, Micikevicius *et al.* [214] maintain a single-precision copy of weights to prevent information loss caused by quantification. Thus they preserve gradient values with small magnitudes and result in half-precision arithmetic. Huang *et al.* [127] proposed the adaptive precision training (APT) method to balance energy cost, memory usage, and accuracy in DL training. Motivated by [215], they find that starting DL training with low precision benefits energy and memory savings. APT dynamically allocates layer-wise bit precision, allowing model to learn faster. Because once the training curve reaches a plateau, increasing precision allows DL training to approach better accuracy with fewer training epochs. And it uses an application-specific hyperparameter to balance the abovementioned three metrics automatically. Wang *et al.* [216] find that during the backpropagation in training, mainly the activation maps' low-frequency component (LFC) is used. As such, they preserve the high-precision copy of LFC while compressing the high-frequency component (HFC) into a low-precision copy. This greatly reduces memory cost while not dramatically decreasing the precision of backpropagations. To realize DL training quantization on MCUs lacking DL training frameworks and low-bit width APIs. Yu *et al.* [217] deploy sub-byte models on MCUs efficiently. They propose a training framework for low-precision models, followed by direct buffer convolution and packed sub-byte multiply-accumulation to accelerate on-device training. Lin *et al.* [38] proposed quantization-aware scaling to alleviate the gradient scale mismatch issues caused by mixed bit-precision training. They stabilized the quantized training by calibrating the gradient scales for MCUs. Instead of improving the quantizer functions, Lu *et al.* [218] optimize the training process from a weight-searching standpoint.

b. Efficient model architecture. DL model compression is another promising method to optimize the AIoT system performance for DL training. Bulo *et al.* [116] proposed in-place activated batch normalization (BN) that eliminates intermediate results and recovers required information during the backward pass, leading to a 50% reduction in memory usage. It can be easily applied on existing models (*e.g.*, ResNet [219], DenseNet [220]) with a minor increase (about 2%) in training latency. Besides, Jung *et al.* [117] split the BN layer into two sub-layers to restructure BN layers. Because existing memory access optimization approaches, such as fusing convolution layers, are ineffective for accelerating BN due to their inability to optimize mini-batch-related calculations during training. To significantly reduce main memory accesses and optimize calculations related to mini-batch, they combined the first sub-layer with the preceding conv layer and the second sub-layer with the following conv layer. To reduce memory usage, some studies also proposed new model structures. *e.g.*, tiny-transfer-learning (TinyTL) [112] added the lite residual module with low-dimensional features and group convolution to improve the model's migration ability. And it avoids intermediate activation storage by only training bias and lite residual modules. This approach leads to a reduction in training memory costs at near-constant precision. Yang *et al.* [209] proposed a reprogramming network, which trains the model using the new task data to reprogram the intermediate features of a backbone model, leading to lower training memory and higher accuracy.

c. Sparse updating. Like pruning in the inference phase, sparse updating does not change the model structure but selects a part of the network to update in each training epoch. Most pruning studies focus on DL inference and are unsuitable for DL training. Liu *et al.* [118] utilize dynamic and sparse graphs (DSGs) in DL training, activating a few neurons during each iteration, resulting in considerable memory savings with competitive accuracy. Dai *et al.* [119] proposed SparseTrain, which employs a stochastic pruning algorithm for each layer and a sparse architecture with 1-dimensional convolution dataflow to realize implicit and artificial sparsity for training acceleration. Lin *et al.* [38] skipped the gradient calculation of insignificantly necessary layers and tensors. And they achieved the near-optimal solution with sparse updating through an evolutionary search. Kaplan *et al.* [221] presented SubTuning, which only trains a carefully selected subset of layers depending on the fine-tuning profile while freezing the remaining. They proved that SubTuning fastly obtains training convergences and even outperforms full fine-tuning when training data is lacking.

2) Model-adaptive system scheduling level: It further maximizes system performance and resource efficiency beyond the optimization capabilities of the algorithm-level techniques and thus pushes the limit of performance-resource tradeoff. As shown in Table IV, it optimizes the intermediate activation tensors and operators in the computation graph, optimizes the runtime/compiler of the DL frameworks, and re-allocates memory/computing resources.

a. Recomputation. In DL training, the intermediate activations generated during the forward propagation are typically stored until the backpropagation to calculate the gradient, which causes a large memory footprint. Experiments have shown that model's intermediate activations use much more memory than parameters [112]. To this end, recomputation methods [120], [121], [223] discard part of intermediate activations right after forward computation to save memory usage and recalculates these activations during backpropagation for gradient calculation, as shown in Figure 22. Chen *et al.* [120] is the first to present the recomputation technique, which splits the model into several parts and keeps only the first activation of each part after forward computation. During backpropagation, activations within each part are computed from the first activation retained. This work realizes significant memory savings. And the recompense of computing delay for memory space is also beneficial, especially when sufficient computing power is available. Following it, Gruslys *et al.* [222] use dynamic programming to find a storage strategy that optimizes computational cost for a given memory budget. Gomez *et al.* [121] applied recomputation in ResNets to save memory footprint during backpropagation. These recomputation methods were mainly implemented on cloud servers with sufficient computing power. The recomputation operations may bring unacceptable additional latency overhead for devices such as Raspberry Pi and MCUs. [141], [224] apply recomputation strategies on mobile phones, using slight additional latency in exchange for significant memory savings.

b. Intermediate activation encoding. Similar to but different from recomputation, intermediate activation compression

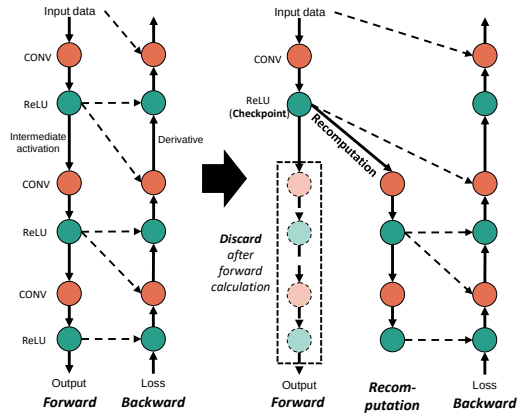


Fig. 22: Illustration of recomputation technique. The intermediate activation is discarded after forward computation and recalculated before backpropagation.

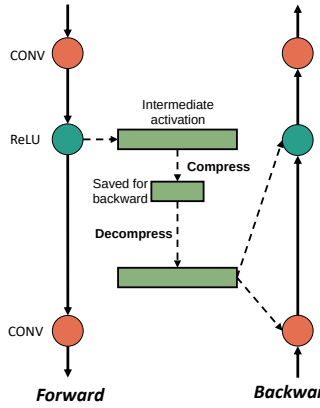


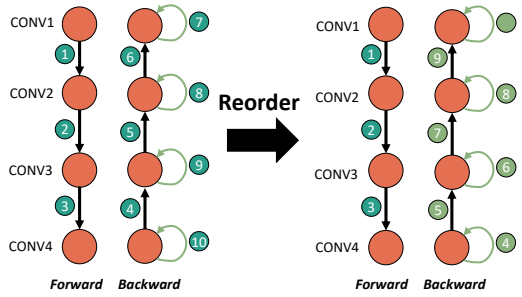
Fig. 23: Illustration of intermediate activation encoding technique. Intermediate activation is encoded after forward computation and decoded during backpropagation.

does not directly discard intermediate activations but *temporarily encode* activations after forward propagation and then *decode* them during backpropagation to calculate gradients, as shown in Figure 23. It thereby strikes a valuable balance between computing latency and memory savings rather than simply trading latency for memory resources. Specifically, Jain *et al.* [122] proposed Gist, a system that employs layer-specific encoding schemes, lossless and lossy, to significantly reduce the memory consumption of targeted feature maps. They store an encoded representation of feature maps and decode them for use in the backward pass; the full-fidelity feature maps are used in their forward pass and relinquished immediately. Evans *et al.* [225] proposed JPEG for activations (JPEGACT), a lossy activation offloading accelerator. They expand the well-known JPEG algorithm for 2D image encoding to compress model's activation. And recently, Hosny *et al.* [226] proposed BitTrain, a novel bitmap compression technique using activation sparsity to reduce the memory footprint during training.

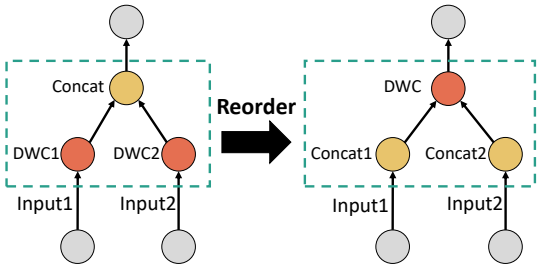
c. Operator reordering. The traditional DL training process retains every gradient in the backpropagation and updates weights uniformly after calculating all gradients. Re-ordering

TABLE IV: Summary of model-adaptive system scheduling techniques for on-device DL training.

Category				Highlight technique for improving resource efficiency	Year	Ref.	Compiler frontend	Compiler backend
Model-adaptive system scheduling level	Computation graph level	Intermediate activation	Recomputation	Split model and only retain part of activations, reduce memory usage with extra computation cost	2016	[120]		✓
				Use dynamic programming in recomputation, optimize computation cost	2016	[222]		✓
				Recomputation for ResNets, reduce memory usage with extra computation cost	2017	[121]	✓	
				Dynamic tensor rematerialization, reduce memory usage with less computation cost	2020	[223]		✓
				Memory-calibrated progressive recomputation on mobile phone, reduce memory usage	2022	[141]		✓
				Progressive recomputation based on memory worthiness of tensors, reduce memory usage	2022	[224]		✓
			Compression	Two Layer-specific encoding schemes, lossless and lossy, reduce memory usage with extra latency	2018	[122]	✓	
				Optimized JPEG method for activation compression and accelerator, reduce memory usage with extra latency	2020	[225]		✓
				A bitmap compression technique using activation sparsity, reduce memory usage with extra latency	2021	[226]	✓	
		Operator	Reordering	Discard gradients, reduce memory usage	2022	[38]	✓	
				Re-order operators to reduce the number of complex operators, reduce computation cost	2022	[227]	✓	
			Fusion	Relaxed graph substitutions by a backtracking search algorithm, reduce execution time and memory usage	2019	[124]		✓
				Transferable deep reinforcement learning for searching, reduce execution time	2020	[125]	✓	
				Account for memory access constraints, a unified memory function, reduce execution time	2020	[228]	✓	
				Merge memory-intensive operators into large GPU kernels, reduce execution time	2020	[229]		✓
				Reduce data movement in memory for Transformer, reduce execution time	2021	[230]		✓
				Consider multiple optimization objectives for memory-intensive computations, reduce latency	2022	[231]		✓
	Resource scheduling level	Memory allocation		Split tensor into micro-tensor to allocate and swap memory, reduce memory usage and latency	2019	[232]		✓
				Tensor life cycle computation and memory sharing, reduce memory usage	2022	[114]		✓
				Tensor-lifetime-aware memory allocation algorithm, reduce memory usage, energy cost, and latency	2022	[141]		✓
		Memory swapping		The first work on DL memory swapping between host(CPU) and device(GPU), reduce memory usage	2016	[39]		✓
				Dynamically select convolution operators and memory swapping strategy, reduce device memory usage	2018	[126]		✓
				Combine recomputation and memory swapping, reduce memory usage	2018	[40]		✓
				Use categorized topological ordering to simulate graph execution, reduce memory usage	2019	[233]		✓
				Decrease amount of synchronization operations and memory offload decisions, reduce memory usage	2019	[234]		✓
				Joint optimization on operator scheduling, memory allocation, and swap decisions, reduce memory usage	2020	[185]		✓
				Memory management based on dynamic tensor access pattern, reduce device memory usage	2020	[191]		✓
				Optimize tensor management on heterogeneous memory, reduce memory usage	2021	[235]		✓
				Selectively compress tensors before memory swapping, reduce memory usage	2021	[236]		✓
				Memory swapping without high-level information of computation graphs, reduce memory usage	2022	[237]		✓
				Improve prefetching using correlation tables to speed up memory swapping, reduce memory usage	2023	[238]		✓



(a) By modifying the operator's execution order, the gradient of each layer is discarded immediately after the weight is updated.



(b) Reording operator can also decrease the number of computation-intensive operations.

Fig. 24: Illustration of operator reordering technique.

operators within the computation graph during backpropagation can reduce peak memory usage [38]. Lin *et al.* [38] proposed the Tiny Training Engine (TTE) to reorder operators in DL training. As shown in figure 24a, by modifying the order of operator execution(exchanging gradient computation and updating operations) in back-propagation, TTE discards the i^{th} gradient immediately after updating the i^{th} layer instead of keeping it throughout the whole training iteration to achieve memory saving. Immediately freeing up space occupied by useless tensors benefits memory savings. Besides, Unity [227] not only changes the operator order but also reduces the number of computation-intensive operations. As shown in figure 24b, Unity exchanges the order of two parallel *Depthwise Conv* (DWC) operators and a *concat* operator to reduce the computation of the convolution process by reducing one DWC operator.

d. Operator fusion. Operator fusion in DL training focuses on merging multiple operators into one to boost computation and memory access efficiency. Suppose two adjacent layers (i^{th} and $i+1^{th}$ layer) in the computational graph are merged, the intermediate activation generated by the i^{th} layer can be directly applied to the $i+1^{th}$ layer without additional read and write transactions with the memory. As a separate note, the *computation graph optimization* that *operation fusion* techniques belong to is a broad field. Various operator fusion techniques have been well explored in existing research [11], [239] and DL frameworks, *e.g.*, TensorFlow [82], PyTorch [176], NCNN [240], and MindSpore [241]. Since fixed rule-based operator fusion cannot guarantee that the performance (*e.g.*, latency) is always optimal [9], [82], [83], MetaFlow [124] realized relaxed graph substitutions for operator fusion via a backtracking search algorithm to address this issue. Zhou *et al.* [125] proposed a transferable deep reinforcement learning-based optimizer to search for optimization policies to improve the optimization efficiency further. It speeds up the search drastically by making decisions based on the entire graph rather than on each node individually compared to previous techniques such as Hierarchical Device Placement(HDP) [242], Spotlight [243], and Placeto [244].

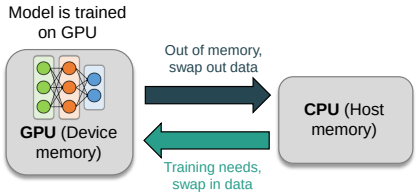
The operator fusion for computation graph optimization can also derive novel DL *compilers* or *frameworks*. For example, Zheng *et al.* [229] introduced a DL training compiler. It merges memory-intensive operators with data dependencies and non-homogeneous parallelism into large GPU kernels, reducing global memory access and context switch overhead. Hu *et al.* [228] proposed Jittor, a just-in-time (JIT) compiled DL framework. It integrated with enhanced operator fusion rules which accounts for memory access constraints as a unified function, allowing for unified management of the GPU memory. Ivanov *et al.* [230] reduced data movement for the Transformer by constructing a dataflow graph, identifying opportunities for data reuse and applying tailored fusion rules. Zheng *et al.* [231] proposed AStitch, a compiler that explores the new operator-stitching optimization space for memory-intensive computations.

e. Memory allocation. Memory allocation methods are typically implemented in the compiler backend, which is closer to hardware resources than the aforementioned techniques for optimizing computation graphs. In DL training, the time between the creation and final access of a tensor is referred to as the tensor's "life cycle." Existing DL frameworks divide a separate memory space for each tensor in the training time, much larger than most tensors' life cycles. Actually, it is useless to keep memory space for the tensor outside its life cycle [114]. Recycling memory for tensors by allocating the same memory for two tensors whose life cycles do not intersect can save memory usage, as shown in Figure 14. Moon *et al.* [114] analyzed all tensors (including input data, weights, and intermediate activations) that may appear during the training time and realized memory recycling, greatly reducing memory usage. Wang *et al.* [141] identified the memory allocation optimization problem is a 2DSP-like NP-hard problem [245]. Since tensors' life cycles can significantly impact layout effectiveness, they positioned long-lifecycle tensors beneath short-lifecycle ones to approximate the ideal solution to this problem. Nie *et al.* [232] presented TSPLIT, a fine-grained model memory allocation method that overcomes memory constraints while retaining DL training efficiency. With the tensor-splitting primitive, TSPLIT breaks the operation boundary of a tensor, allowing flexible memory allocation.

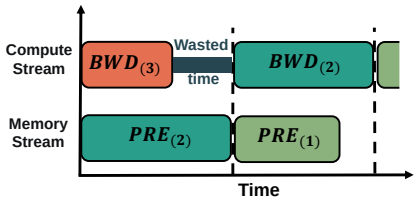
f. Memory swapping. In DL training, the intermediate activation of a certain model layer is *temporarily used* in the layer's forward and backpropagation. Swapping temporarily unused intermediate activations from the precious memory (*e.g.*, GPU) to the larger memory (*e.g.*, CPU) and then swapping back when gradient updating needs them can speed up computation and reduce memory usage, as shown in Figure 25a. Memory swapping is commonly supported by *operating systems*, *e.g.*, virtual address spaces in Windows [246] and

TABLE V: Summary of related intra-device controllers for on-device DL training.

Category	Focus level	Context awareness	Controller	Optimized performance	Year	Ref.
Controller level	Resource-friendly algorithm level including quantization	Gradient, energy, memory	/	Layer-wise quantified precision	2020	[127]
	Model-adaptive system scheduling level including checkpoints in computation graph	Memory budget	Dynamic programming	Total computational cost	2016	[222]
	Model-adaptive system scheduling level including checkpoints in computation graph	Tensor staleness, memory budget	Greedy, heuristics	Total computational cost	2020	[223]
	Model-adaptive system scheduling level including memory swapping	Memory budget	Genetic algorithm	Execution time	2020	[185]
	Model-adaptive system scheduling level including memory swapping	GPU architecture	Bayesian optimization	(De)Compression time	2021	[236]
	Co-design: resource-friendly algorithm level including quantization, sparse updating & model-adaptive system scheduling level including operator reordering	Memory budget	Evolutionary search	Accuracy	2022	[38]



(a) Memory swapping process.



(b) Memory swapping delay.

Fig. 25: Illustration of the memory swapping technique. $BWD_{(n)}$ and $PRE_{(n)}$ are the backward and prefetch computations for $layer_{(n)}$, respectively.

swaps partitions in Linux [247]. When the memory capacity of a device is insufficient, data will temporarily swap out to external memory like disks. However, it brings extra transfer delay. And memory usage is difficult to predict for random programs. Notably, this shortcoming can be well solved in DL training because the forward computation and backpropagation are in fixed orders (*i.e.*, forward computation from the first layer to the last layer and backpropagation is contrary), bringing optimization potential to memory swapping. For example, the data d^2 required by $layer_2$ backward propogation $BWD_{(2)}$ can be prefetched to GPU memory during $BWD_{(2)}$ computation. As a result, the d^2 transfer delay $PRE_{(2)}$ can be partially covered by $BWD_{(3)}$, or completely coverd like $PRE_{(3)}$, as shown in figure 25b.

Rhu *et al.* [39] proposed vDNN, the first work on memory swapping for DL training. They propose a runtime memory manager that virtualizes the memory utilization of models by enabling the concurrent usage of both GPU and CPU memory during training. vDNN reduces the average GPU memory usage of multiple mainstream models by over 90%. Following vDNN, Chen *et al.* [126] proposed moDNN, an intelligent solution capable of dynamically choosing convolution operators, adjusting mini-batch size, and selecting the suitable memory-swapping strategy to achieve optimal system performance. It realized fast Fourier transforms and Winograd with improved performance and increased memory requirements. Subsequently, Wang *et al.* [40] combined the memory swapping and recomputation methods and realized dynamic GPU memory scheduling that enabled DL training far beyond the GPU DRAM capacity. Le *et al.* [233] formally rewritten the computation graph and inserted swap-out and swap-in operations to store intermediate results on CPU memory. By introducing a categorized topological ordering to simulate computation graph execution, the memory consumption of a model can be profiled using operation distances in the ordering. Shriram *et al.* [234] proposed vDNN++ t o address the issues of delayed computation start, high pinned memory requirements, and GPU memory fragmentation in vDNN [39] by lowering the number of synchronization operations. Huang *et al.* [185] proposed SwapAdvisor to enhance the previously presented memory swapping methods with manual judgment. It jointly optimizes three dimensions of given dataflow graphs, *i.e.*, operator scheduling, memory allocation, and swap decisions. SwapAdvisor explores the wide search space through a genetic algorithm, improving the GPU's capability to accommodate large models, *e.g.*, WideResNet-152 [155], NasNet-25 [248], and BRNN-4-8K [249], they need 180GB, 193GB, and 99GB memory space for training, respectively. Following it, Peng *et al.* [191] conducted flexible memory management control by dynamically tracking the tensor access patterns at

runtime, which decide when and how to swap memory.

Furthermore, Ren *et al.* [235] presented Sentinel, a runtime system that automatically optimizes tensor management on heterogeneous memory. Specifically, it enables the optimal memory *co-allocation* for several tensors with similar lifetime and memory access frequencies by allocating them to the same pages to avoid unnecessary data movement. Then Chen *et al.* [236] optimize memory swapping time by selectively compressing tensors based on their sparsity, and size. Li *et al.* [237] automatically trace the memory behaviors of model workloads to schedule memory swapping without perceiving high-level information of layer structures or computation graphs, which alleviate the problem of existing solutions being densely coupled with the fixed model workloads, *e.g.*, layer structures or computational graphs. Jaehoon *et al.* [238] presented DeepUM, offering GPU memory oversubscription for models by leveraging compute unified device architecture (CUDA) unified memory and employing CPU memory as a backing store. They used a new correlation prefetching mechanism at UM block level to hide the fault-handling overhead. Thus it considerably reduces memory swapping time and increases GPU's virtual memory capacity.

3) Intra-device cross-level controller: The resource demands of DL training tasks vary. This variability, combined with the heterogeneous computing/memory resources of AIoT devices, can provide numerous optimization possibilities. For instance, when a device has tight memory and rich computing resources, it may be necessary to frequently employ recomputation techniques, while for a device with sufficient memory, such strategies can be avoided to reduce unnecessary computation delay. Furthermore, different training epochs on the same device can result in diverse performance outcomes. Therefore, an adaptive controller should be employed in the resource-efficient AIoT system to adjust the technique configuration based on the availability of resources and performance demands. A context-aware controller can prevent memory units from being idle or overloaded, thereby enhancing efficiency.

Table V summarizes existing adaptive controllers integrated with diverse levels of optimization techniques. For example, Huang *et al.* [127] proposed adaptive precision training in DL training quantization. It dynamically allocated layer-wise precision and provided an application-specific hyperparameter for users to achieve the trade-off between training energy cost, memory usage, and accuracy. In sparse updating, Lin *et al.* [38] adopted an evolutionary algorithm to search for the most important layers for updating and achieve higher training accuracy under a limited memory budget. In recomputation, Gruslys *et al.* [222] utilized dynamic programming to balance intermediate activations and recomputation caching. With a tunable memory budget, it can optimize computation costs. Kirisame *et al.* [223] extended recomputation methods by introducing dynamic tensor rematerialization (DTR). DTR is a greedy online algorithm that is parameterized by eviction policy. In memory swapping, Huang *et al.* [185] proposed SwapAdvisor, which uses a genetic algorithm to search for the optimal memory swapping scheme for reducing the transfer delay between CPU and GPU memory. Given the memory budgets, they used a dataflow engine simulator to quickly estimate the execution time of each scheme and find the best one with the lowest latency. Chen *et al.* [236] proposed a self-tuning tensor compression framework CSWAP. It used bayesian optimization to search for the optimal hyperparameters for tensor compression and tackle the heterogeneity caused by different GPU device architectures and DL frameworks.

B. Distributed DL Training

With the increase in DL model complexity and diversity, training models on AIoT devices at low cost is still challenging. To realize this intractable goal, distributed DL training on multiple AIoT devices is considered as the promising way [133], [250], [251]. This includes centralized systems such as model ensembling [252], decentralized systems such as tree-like topology [253] and parameter server [254], and fully distributed systems such as peer-to-peer [255]. Distributed DL training (with/without privacy concerns) partitions the data or DL models, reducing the memory load on each device compared to on-device training (as discussed in § IV-A).

Existing effort on distributed DL training (without privacy concern) mainly includes three categories, *i.e.*, model parallelism, data parallelism, and hybrid parallelism. Figure 27a shows their difference. When the DL model is too large to feed into a single device, it is necessary to adopt *model parallelism* to assign different parts of the model to diverse AIoT devices for training and finally merge them into a complete model. *Data parallelism* divides huge data into N parts to deploy N distributed AIoT devices without privacy concerns. Each AIoT device only processes $1/N$ of data and aggregates gradients to the central server for an update. *Hybrid parallelism* combines the strengths of the above two schemes. Federated learning is a widely known data parallelism method with privacy concerns. And in AIoT federated learning, the data on each AIoT device is sensed by itself and cannot be re-distributed. It only shares the model updates among multiple devices. Federated learning includes asynchronous, semi-synchronous, and synchronous schemes, as shown in Figure 27b. In this section, from the cross-level perspective of a resource-efficient AIoT system, we introduce enabling techniques at different levels, *i.e.*, resource-friendly algorithm, model-adaptive system scheduling, and inter-device controller upon them, illustrated in Figure 26.

1) Resource-friendly algorithm level: At the algorithm level, researchers explore partitioning the DL models for training parallelism or scheduling various devices in parallel to improve training efficiency. Federated learning is one of the widely-used distributed learning schemes. To reduce waiting time, Xie *et al.* [257] used asynchronous federated learning technology, adopting an asynchronous collaboration mode of upload-on-the-fly to minimize training time for each round. Then Ouyang*et al.* [259] proposed a novel federated learning system that can identify intrinsic similarities between data points, leading to higher model accuracy and lower communication overhead. In distributed learning without privacy concerns, Huang *et al.* [128] proposed GPipe, a scalable model parallelism library to boost the training efficiency of giant models, *e.g.*, generative pre-trained transformer (GPT) and bidirectional encoder representations from transformers

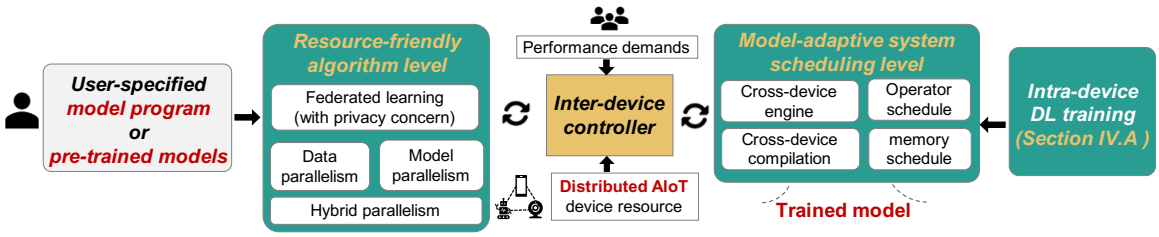
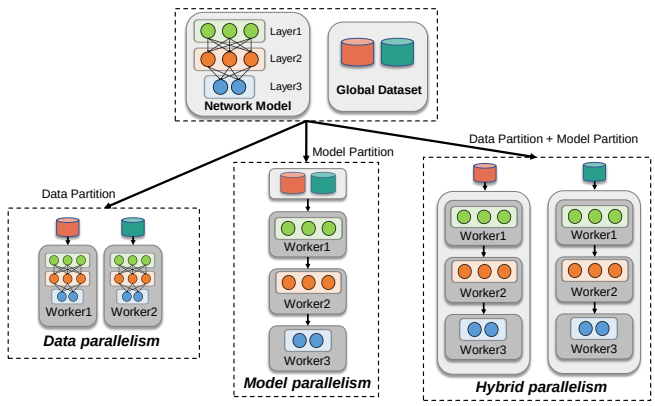
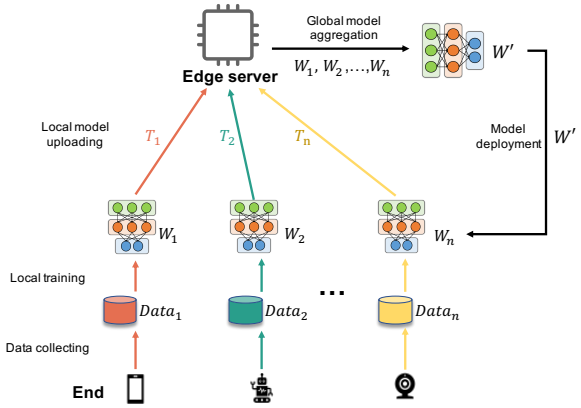


Fig. 26: System loop of the algorithm, system scheduling, and inter-device controller for distributed DL training.



(a) Distributed DL training (without privacy concern)



(b) Federated learning (with privacy concern)

Fig. 27: Illustration of different distributed DL training techniques. (a) Distributed learning (without privacy concerns) can be divided into data parallelism, model parallelism, and hybrid parallelism; (b) Considering different time points of model updating, federated learning includes asynchronous, semi-synchronous, and synchronous schemes.

(BERT). GPipe partitioned the model across different accelerators and split the mini-batch into smaller micro-batches for parallelism execution. By splitting batch, GPipe provided an almost linear speed up, *i.e.*, $3.5 \sim 20\times$, with no alterations to the model parameters. PipeDream-2BW [250] realized the memory-efficient DL training parallelism by utilizing a new weight gradient coalescing algorithm and weight double buffering. It efficiently split the DL model across available hardware resources considering hardware limits such as accelerator memory capacity and interconnect topologies. Beaumont *et al.* [256] proposed MadPipe to dramatically improve the training throughput by hybrid parallelism. It gives a more precise estimation of the memory requirements and a dynamic programming-based heuristic algorithm, which results in efficient computation-memory allocation and schedule.

2) Model-adaptive system scheduling level: It is intractable to enable the scalability and adaptivity of the distributed DL training to fully use varying resources in AIoT devices (*e.g.*, drone swarms and smart camera arrays) whose resources dynamically change due to the influence of other on-device tasks. Cui *et al.* [130] proposed GeePS, the first GPU-specialized *parameter server* design for realizing the data-parallel DL training on GPUs. Compared to previous CPU-based parameter server systems, GeePS employs GPU-friendly caching, data staging, and memory management techniques to reallocate GPU memory for intermediate layer state cache, significantly reducing training latency. Wahib [131] proposed a performance model based on the concurrent analysis of out-of-core training behavior and combined layer-wise memory swapping and redundant recomputing to decrease memory usage during training. Regarding scalability, the proposed out-of-core data parallel method outperforms complicated hybrid model parallelism in training huge models, *e.g.*, Megatron-LM [262] and Turning-NLG [263]. Rajbhandari *et al.* [260] proposed a zero redundancy optimizer (ZeRO) to optimize memory usage and improve distributed training speed while increasing the model size. ZeRO mainly employs two techniques, *i.e.*, reducing memory state redundancy across data-parallel processes by splitting the model states rather than repeating them; and proactively allocating memory based on the lifetime of various tensors to prevent memory fragmentation.

Md *et al.* [261] proposed DistGNN, which uses a minimum vertex-cut graph partitioning algorithm to reduce the transfer time of features and gradients. DistGNN further accelerates the shared memory system by using cache blocking, loop reordering, and vectorization with the LIBXSMM library [264], which considerably boosts distributed training throughput. Then Lim *et al.* [132] proposed Zico, the first model system which aims to reduce the memory consumption for parallelism training. Zico monitors the memory usage of each training task through its progress on GPU computation and reclaims the memory that is no longer needed, making it globally sharable. As a general approach, Zico outperforms existing GPU-sharing methods. Recently, Liu *et al.* [251] presented MAP, a PyTorch-

TABLE VI: Summary of cross-level optimization techniques for distributed DL training.

Category		Highlight technique for improving resource efficiency	Year	Ref.	Parallelism mode		
					Data	Model	Hybrid
Resource-friendly algorithm level	Distributed DL training (without privacy concern)	Compute layers in pipeline to reduce latency caused by distributed training	2019	[128]		✓	
		Pipelining and weight gradient coalescing to reduce memory usage and latency	2021	[250]			✓
		Dynamic programming based heuristic to estimate memory requirements more precisely, reduce latency	2022	[256]			✓
	Federated learning (with privacy concern)	Asynchronous federated learning to minimize waiting latency	2019	[257]	✓		
		Re-parameterization to decrease the convergence time	2020	[258]	✓		
		Similarity-aware federated learning system to reduce communication overhead	2021	[259]	✓		
Model-adaptive system scheduling level		First GPU-specialized parameter server, reduce latency	2016	[130]	✓		
		Layer swapping and recomputing; out-of-core training behavior analyzing, reduce GPU memory usage	2020	[131]	✓		
		Eliminating memory redundancies with Zero Redundancy Optimizer, reduce memory usage	2020	[260]			✓
		Shared memory, minimum vertex-cut graph partitioning algorithm, delayedupdate algorithms. Reduce latency	2021	[261]	✓		
		Sharing global memory among concurrent jobs, reduce training time	2021	[132]			✓
		A symbolic profiler to estimate memory and computing statistics to improve distributed training efficiency	2023	[251]			✓

TABLE VII: Summary of related inter-device controllers for distributed DL training.

Category		Focus level	Context awareness	Controller	Optimizated performance	Year	Ref.
Inter-device controller level	Federated learning (with privacy concern)	Resource-friendly algorithm level including data distribution and device training latency	Heterogeneous device resources, sample importance	Greedy heuristic	Training time	2021	[265]
		Resource-friendly algorithm level including device conditions	Network bandwidth, heterogeneous devices	Synchronization scheduler	Energy consumption, training time, accuracy	2022	[266]
	Distributed learning (without privacy concern)	Resource-friendly algorithm level including device conditions	Network throughput, computing resources	/	Energy consumption, training time	2022	[133]
		Resource-friendly algorithm level including memory estimation and non-contiguous allocations of DL layers	Memory budget, network bandwidth	Dynamic programming	Execution time	2022	[256]
		Model-adaptive system scheduling including checkpoints in computation graph	Memory budget	Markov Chain Monte Carlo search algorithm	Execution time	2020	[267]
		Model-adaptive system scheduling including checkpoints in computation graph	Memory budget	Dynamic programming	The number of recomputation	2020	[268]
		Model-adaptive system scheduling including model statistics collection and computation graph static planning	Memory budget	/	Execution time	2023	[251]

based compiler that implements memory-aware automated parallelization and provides near-real-time memory and computing statistics. MAP can build distributed execution plans with high training efficiency. Because it involves a symbolic profiler to swiftly collect memory and computation overhead, a cluster detector to gather cluster hardware performance and topology, and a tense layout manager.

3) Inter-device cross-level controller: Like on-device DL training, distributed DL training also benefits from the context-aware controller. On the one hand, imbalances in completion time among different devices result in significant synchronization overheads. On the other hand, DL training parallelism depends on the degree of the decoupled model layer, channel, or operator. Table VII summarizes some prior explorations. In federated learning, the disparate computational capabilities of the devices involved can result in differences in training time, which can impact the overall system efficiency. Lai *et al.* [265] introduced Oort, a method that enhances the performance of federated training and testing through guided participant selection. Oort employs a synchronous federated learning scheme, selecting participants with similar device performance for training in each round to mitigate the impact of hardware differences among devices. To further reduce the impact of heterogeneous devices, Sun *et al.* [266] proposed FedSEA, a semi-asynchronous FL framework for extremely heterogeneous devices. FedSEA adjusts training parameters for device heterogeneity and balances the trade-off between waiting costs and data benefits. MemFlow [267] jointly optimizes memory usage and computation time when searching for an optimal parallelism training strategy. In detail, it adopts a Markov chain monte Carlo search algorithm to select the most suitable degrees of recomputation. Olivier *et al.* [268] employed memory-aware scheduling and automatic differentiation to execute a back-propagation graph within the bounded memory requirement at the cost of computation.

Recently, Liu *et al.* [251] proposed MAP to search for the optimal distributed training strategy in two ways, *i.e.*, intra-operator parallelism and activation checkpoint. Also, to automate intra-operator parallel training for large models, MAP adopted an efficient strategy using a two-stage solver and recompiled it into a module instance. However, the cross-level adaptive controller in a broader space for distributed DL training is still underexplored. According to the dynamically available resources of different AIoT devices in the distributed system without privacy concerns, the split data and model sizes can be dynamically adjusted for diverse devices. To better

TABLE VIII: Comparison of two types of resource-efficient DL engines for AIoT.

Type	Engine	DL model parser	DL model interpreter	DL model optimizer	DL model compiler
Compiled engine	TVM [9]	✓	✓	✓	✓
	OneDNN [35]		✓	✓	✓
	TensorflowXLA [11]	✓		✓	✓
	TensorflowRuntime [10]	✓		✓	✓
Interpreted engine	TensorflowLite [26]	✓	✓	✓	
	CMix-NN [34]		✓	✓	
	CMSIS-NN [269]	✓	✓	✓	

control different devices' training cycles and synchronization strategies, Samikwa *et al.* [133] introduced resource-aware split-learning (ARES) for adaptive DL distributed training. ARES presented the device-oriented model partition method, which adaptively deploys tasks for heterogeneous devices to reduce the impact of stragglers. To address insufficient memory issues on individual end devices, Beaumont *et al.* [256] uses a dynamic programming-based heuristic to find the best strategy for distributed memory allocation.

Discussion. The cross-layer optimization of DL training is essential for achieving efficient and effective AIoT deployments. While both DL training and DL inference (§ III) can benefit from similar optimization approaches and automated controllers, training poses additional constraints and challenges due to higher computational and storage requirements and increased sensitivity to errors. On one hand, both DL training and DL inference share the same cross-layer optimization space and require automated controllers, whether implemented on-device or in a distributed manner. Table IV presents a range of individual optimization techniques that can be employed for DL training task optimization in AIoT systems. Similarly, the performance of optimization techniques can vary significantly, necessitating careful selection and exploration of their combined usage on AIoT devices. On the other hand, DL training has higher computational and storage requirements compared to DL inference, along with increased sensitivity to errors due to multiple iterations. This implies that DL training imposes more constraints and challenges compared to DL inference.

V. Resource-efficient AIoT Applications

This section briefly introduces some enabling systems and the potential application scenarios in AIoT.

A. DL Engines for AIoT

The engine for resource-efficient DL deployment at AIoT devices mainly aims at improving the flexibility of memory scheduling, optimizing the computational efficiency of operators, and enhancing the underlying adaptability to heterogeneous devices. It creates a paradigm shift in how operators are carried out. As shown in Figure 28, they include *interpreted* and *compiled engines*,We demonstrated how these two different deep learning engines play a role in deploying models to devices.

Interpreted engines generally include the DL model parser, interpreter, and optimizer. The DL model parser is responsible for reading and parsing the model file and converting it into a format suitable for processing by the interpreter. The DL model optimizer is responsible for transforming the original DL model into an equivalent model with more efficient inference/training speed; The DL model interpreter accepts the input data from the application scenarios and executes the corresponding internal operators of the DNN in sequence according to the model architecture and target device's hardware schedule configurations to finally output results.

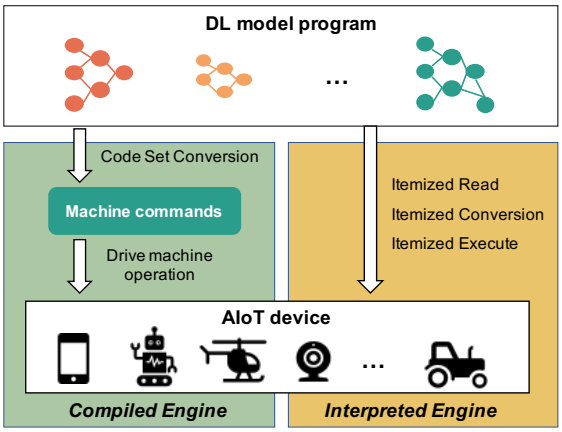


Fig. 28: Difference of interpreted and compiled engines.

Compiled engines mainly involve the DL model parser and compiler. The role of the model parser is the same as that of interpreted engines. The compiler transforms models into machine code that can be directly processed by the target deployment platform (such as CPU, GPU, *etc.* Also, it can apply various optimization methods during the compilation process to improve the operating efficiency of machine codes, such as automatic computing graph scheduling [9].

Table VIII summarizes the state-of-the-art DL deployment engines on AIoT devices. Recent representative compiled inference engines mainly include TVM [9], oneDNN [35], TensorFlow XLA [11], TensorFlow Runtime [10], *et al.*. Different engines focus on different aspects. For example, TVM [9] is a cross-platform DL development framework. Compared with commonly used frameworks such as Tensorflow and Pytorch, TVM optimizes DNN operators at the computation graph level by converting operators into descriptions of tensor changes, generating code, and transmitting it to the CUDA compiler. TVM does not rely on a specific framework's compute library and can be deployed on diverse hardware platforms. Meanwhile, TVM supports integrating new operators. Unlike the cross-platform characteristics of TVM, OneDNN [35] emphasizes on DL performance optimization

with Intel-architecture processors, Intel-architecture graphics cards, and Xe-architecture graphics cards. The oneDNN engine executes DNN primitives to process data in several memory objects, reducing memory usage of DL inference. The primitives are objects encapsulating specific computations, *e.g.*, forward convolution, data transformation, *etc.* Compared to purely functional operations (*e.g.*, conv), primitives can be specialized for a subset of input parameters. Both TVM and OneDNN are compatible with various DL frameworks.

Some other engines are deeply optimized for one framework, such as Tensorflow XLA [11] and Tensorflow Runtime [10]. TensorflowXLA [11] is a linear algebra compiler engine for the TensorFlow framework. In the regular TensorFlow framework, when a program runs, it invokes a pre-compiled GPU kernel for each operation, causing the computing kernel redundancy problem. TensorflowXLA solve this problem by compiling the computation graph of each DNN into a series of specially generated computation kernels to speed up DL inference and improve memory usage with model-specific information. Tensorflow Runtime (TFRT) [10] mainly optimizes the DL inference for specific hardware in various fields to enable scalability. It implements efficient execution of the computing kernel through specific primitives on the underlying devices. Meanwhile, it optimizes the parallel operation of the existing graph and reduces the synchronization overhead. Also, TFRT provides a lightweight just-in-time operator distribution stack for asynchronous API calls to improve computing efficiency.

TFlite [26] is a lightweight engine that is mainly applied to DL inference on mobile devices. TFlite not only provides a series of core operators according to the requirements of mobile platforms but also supports custom operators. And TFlite defines a new DNN file format, removing the parsing step before revisiting data, and greatly reduces the memory footprint of the code. In addition, TFlite designed an optimized interpreter that uses static graphic sorting and a custom (less dynamic) memory allocator to ensure minimal load, and execution latency. CMix-NN [34] is a framework specifically supporting DNN inference on MCU. Compared with other frameworks, CMix-NN focuses on effectively compressing DNNs. Specifically, CMix-NN supports DNN quantization strategies for diverse DNN layer, filter channel, and activation. CMSIS-NN [269] is an edge DNN inference framework for the internet of things (IOT) scenarios. It can directly interact with the underlying hardware, improving computing efficiency by up to $5\times$ in the MCU tests.

Discussion. Building upon the aforementioned techniques, engine systems can assist the algorithm layer in achieving cross-layer optimization of AIoT systems. Compiled engines offer advantages such as reduced memory consumption and simplified deployment, while interpreted engines excel in adapting to various hardware architectures at runtime. The choice between them depends on the specific requirements and constraints of the AIoT system. Compiled engines, with their lower memory footprint and absence of additional graph interpretation, offer improved support for heterogeneous AIoT devices. However, their runtime and dynamic adaptation capabilities remain limited. On the other hand, interpreted engines excel in executing DL inference and training tasks across diverse AIoT devices. They possess the ability to interpret the computation graph based on specific hardware instructions during runtime. This flexibility allows for efficient utilization of the underlying hardware resources, enabling optimal performance across different AIoT device configurations.

B. Resource-efficient AIoT system for Diverse Applications

The remarkable success of DL has fostered a growing number of intelligent applications/services on AIoT devices [248], [282]–[285]. Table IX summarizes three typical AIoT applications, *e.g.*, image classification, semantic segmentation, and speech recognition. And we note that the algorithm-system co-design that jointly optimizes the resource-friendly DL models and model-adaptive resource scheduling can improve the runtime resource availability and thus pushes the limit of performance-resource tradeoff set by standalone levels.

1) Cross-level optimization for image classification: Image classification has a wide range of applications, including object classification [286], human face recognition [287], remote-sensing image recognition [288], image spectrum analysis [289] *etc.* There are many attempts at the algorithm and system scheduling levels. Qian *et al.* [290] proposed the recurrent aggregation operator (ReX) to extract informative information and avoid memory-intensive large-scale early activations. ReX integrates important features of intermediate activations by using two RNNs and compresses them into a low-dimensional vector, which greatly reduces the memory footprint in the early exit module.

2) Cross-level optimization for semantic segmentation: In contrast to image classification, which only requires a single label for the entire image, semantic segmentation requires labels for each pixel. It is the pixel-level segmentation of different objects. Therefore, semantic segmentation is more memory exhaustive than image classification, especially on large images [291]. To realize on-device semantic segmentation on the AIoT device, Jin *et al.* [277] designed an adaptive built-in memory module to decrease memory usage. We note that cross-level algorithm and system scheduling co-design will be beneficial. Wang *et al.* [275] presents Lednet based on an asymmetric encoding and decoding structure. And they designed two new operators, *i.e.*, channel splitting and shuffling, which reduced the computing cost of the entire network and improved the computing speed.

3) Cross-level optimization for speech recognition: Speech recognition has a broad application area, such as smart home [292], [293] and intelligent driving [294], [295]. Diverse studies have investigated compressing memory for various aspects of speech recognition applications, including data separation [296], lightweight models [280], [281], and system deployment [297]. For example, Shangguan *et al.* [278] supported the lightweight conversion of various speech recognition models, such as RNN and LSTM, by integrating different computational graph optimization techniques. Han *et al.* [298] proposed load-balance-aware pruning to ensure high hardware utilization. And they design a system scheduler that encodes the compressed model to multiple PEs for parallelism and schedules the complicated LSTM data flow.

TABLE IX: Summary of resource-efficient AIoT system optimization for enabling diverse resource-aware applications.

Applications	Technique highlight for improving resource efficiency	Focus level	Optimization	Year	Ref.
Image classification	Hyperspectral analysis, less parameters	Computation graph	Improve accuracy	2020	[270]
	Quickly reduce the size of the image	DL model	Reduce parameters	2020	[271]
	Reduce early activation	Operetor	Increase inputs	2021	[272]
	Quantum computing,few memory	Inter-device controller	Reduce data storage	2022	[273]
Semantic segmentation	Space pyramid	DL model	Improve computing speed	2019	[274]
	Asymmetric codec structure	Computation graph	Reduce memory	2019	[275]
	Trapezoidal up-sampling	Operator	Improve computing speed	2020	[276]
	Built-in memory module	Memory scheduling	Improve accuracy	2021	[277]
Speech recognition	End-to-end neural network architecture	Computation graph	Reduce parameters	2019	[278]
	Finite-size beam search decoding	Computation graph	Improve accuracy	2020	[279]
	Low rank matrix substitution	DL model	Reduce parameters	2020	[280]
	Streaming oriented speech separation technology	Inter-device controller	Improve computing speed	2020	[281]

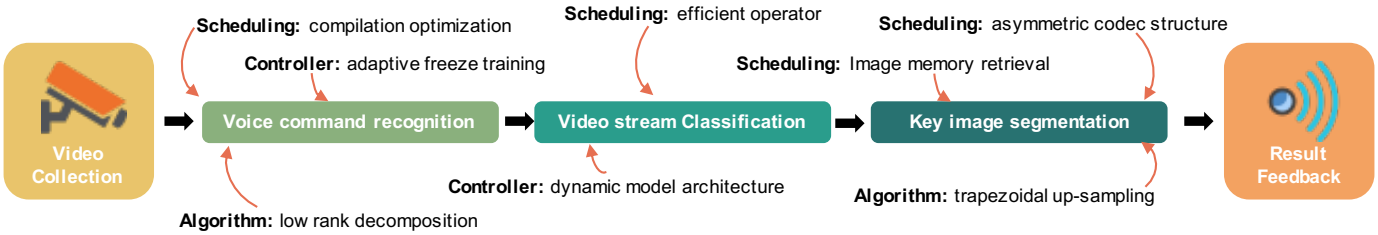


Fig. 29: An example of cross-level optimization for resource-efficient video analysis in smart city scenarios.

4) AIoT-powered application scenarios: Above advances in applications have driven increasing solutions in various AIoT scenarios, including smart homes [299]–[302], smart factories [303]–[305], and smart cities [306]–[308].

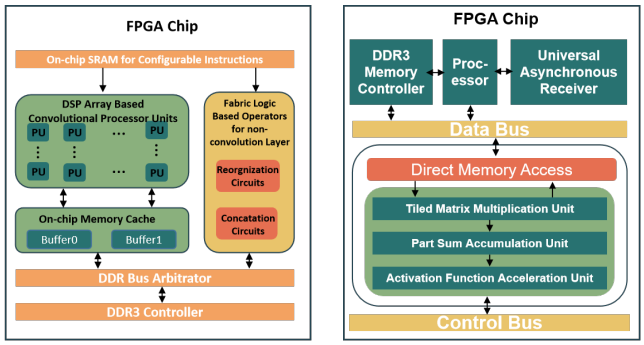
Smart home. Current smart home scenarios involve video/voice recognition and environmental awareness to realize automated appliance operations, *e.g.*, curtain controlling and TV turning on/off. Deeperthings [90] proposed a collaborative optimization framework at three levels: communication, computing, and memory usage. By integrating communication and perception layers to achieve cross-layer overall optimization and balancing memory usage between different devices, the efficient inference is ultimately achieved in resource-constrained situations. Given the diversity and complexity of scenarios, the resource-efficient AIoT system deployed in open environments should dynamically adjust itself. Also, cross-level optimization must be jointly explored.

Smart city. In urban construction and city life, resource-efficient AIoT systems have stimulated plenty of applications, *e.g.*, traffic flow prediction [303], street map estimation [304], and air quality prediction [305]. Specifically, accurate traffic flow prediction serves lane planning [309] and indicator time regulation [310]. As shown in Figure 29, We used monitoring as an example to analyze how optimization technologies at different levels are applied to the systems of smart cities Summarily, resource-efficient AIoT systems in smart cities usually comprise heterogeneous devices with a large physical span. To ensure efficient collaboration, it is necessary to provide unified management of cross-device resources at the algorithm and underlying system levels.

Smart industry. Resource-efficient AIoT systems are gradually integrated into engineering management and process optimization to in the industrial field. The specific functionality includes product defect detection, manufacturing process optimization, predictive operation and maintenance, equipment failure warning, production process planning, *etc.* To avoid the fragmented ecosystem of DL models in AIoT industry, Ren *et al.* [311] proposed a framework using Semantic Web technologies to enable the joint management of TinyML models and IoT devices at scale, from modeling information to discovering possible combinations and benchmarking, and eventually facilitate TinyML component exchange and reuse.

C. Resource-efficient AIoT System on Heterogeneous Devices

Diverse AIoT devices are always heterogeneous regarding memory, computing, and battery resources. And it is non-trivial to deploy resource-efficient AIoT system on heterogeneous devices. Specifically, we select three types of representative AIoT devices, *i.e.*, the cheapest but with extremely constrained MCU devices, the most ubiquitous ARM-based mobile devices (*e.g.*, smartphones, wearables, robots), and typical GPU-based edge servers with weak resources (*e.g.*, NVIDIA DGX, HPE ProLiant DL380 Gen10). As an indispensable interface, smartphones often serve as the control center of AIoT clusters. The MCU is very cheap but has extremely limited computing and memory resources. And the FPGA chip stands out with the advantages of high flexibility, low power consumption, and strong expansibility. Table X summarizes how to optimize resource-efficient AIoT systems in MCU, ARM, and FPGA devices.



(a) DLAU (b) WPU

Fig. 30: Two different FPGA architectures for convolution acceleration, in which DLAU mainly adopts a three-layer pipeline, and WPU uses a sparse network design.

1) Resource-efficient AIoT system on MCUs: MCU is widely used for simple tasks in autopilot, medical care, office equipment, *etc.* And its small size and low cost make it suitable for large-scale deployment, *e.g.*, the daily inspection of the lake surface [312]. However, the MCU's tightly-limited memory resources constrain the efficient execution of DL inference/training tasks. Many studies [12], [71], [123], [226], [313]–[317] have been conducted for DL deployment on MCUs. SpArSe [318] is a network architecture search (NAS) framework designed for DL inference on MCUs. Micronets [313] also leverage NAS for specifying DNN architectures. To map the MCU-imposed memory, latency, and energy constraints to the NAS search framework, they found an important basis, *i.e.*, model latency varies linearly with the model operation (op) counts before searching models in space. And they used these discoveries in NAS to reduce memory utilization and operands. μNAS [71] is another NAS system for MCNS, emphasizing RAM size, memory size, and processor speed. MCUNets [12] integrates Tiny NAS and Tiny Engine to optimize the resource-efficient AIoT systems on MCUs. They find that for a DNN with the same size, the larger the amount of computation, the higher the accuracy. With this insight, Tiny NAS greatly reduces the search space and improves search efficiency. TinyEngine is a compilation engine that reduces the memory occupation in DNN operation by optimizing the loop operation. Facing the huge memory cost of the first few CNN layers, MCUNetsV2 [123] makes longitudinal cutting to execute a small part of models and finally integrate the results of all cut parts.

2) Resource-efficient AIoT system on ARMs: Compared to MCUs, ARM-based devices have more powerful computing power and are widely used in mobile devices such as robots and drones. To accelerate DNN inference/training on ARM devices, many researches [240], [320], [321], [323], [327]–[330] have been proposed. It is reported that the conv layers in DNNs consume most of the computation due to the high computational amount [331]. Huang *et al.* [319] realized the parallel conv computing based on the fast Fourier transform, which optimized the memory occupation and reduced the latency of multi-core parallel. To further improve non-uniform memory access in many-core CPUs, Huang *et al.* [322] proposed a fast Fourier convolution method based on NUMA awareness, conducting data rearrangement and parallelizing complex matrix multiplications to reduce remote memory accesses and thus improves the calculation of CNNs. Meng *et al.* [320] proposed FastConv, a template-based open-source library for automatic code generation, which can automatically generate high-performance CNN kernel and improve the performance of the conv layers on ARM devices. Meanwhile, Li *et al.* [321] focued on maximizing the parallelism of the algorithm to fully utilize the multiple processing cores available on modern ARM CPUs. They propose several optimizations, including a parallel tile processing scheme, a memory layout optimization, and an efficient data rearrangement technique. Zhou *et al.* [323] optimized convolution layers through pipeline strategy. It computed the 3×3 convolution on the ARM CPU by means of a single instruction and multiple data. And it improved the computational efficiency by increasing the data reuse rate. Tencent *et al.* [240] presented NCNN framework, an ARM-based DNN optimization framework that integrates various memory management techniques. It utilizes multi-core parallel to accelerate the DNN calculation. The cross-platform characteristics of NCNN greatly benefit users in transplanting the DL models to the AIoT terminals and reducing the latency and memory occupation of DNNs.

3) Resource-efficient AIoT system on FGPAs: FGPA is developed based on programmable array logic and universal array logic. The main feature of FGPAs is that they are customizable and can independently change the circuit structure and expand the chips according to the amount and way of calculation [203], [324]. When deploying DNNs on FPGAs, such special features can maximize computational efficiency and reduce energy costs. Therefore, in AIoT application scenarios, FPGA is becoming a promising intelligent perception, computing, and control platform [332]. Existing efforts [325], [326], [333]–[336] have begun to study resource-efficient DNN deployments with FGPAs. Wang *et al.* [324] proposed DLAU, a scalable accelerator architecture for the large-scale deployment of DNNs on FGPA. In previous studies, the DL acceleration mainly includes loop unrolling [337], tiling [189], switching [338], *etc.* These methods, however, without hardware redesigning, can hardly give full play to the programmable characteristics of FGPA. To this end, Ma *et al.* [203] designed the specific data stream to accelerate DL execution, as shown in Figure 30(a). To optimize memory accesses, they minimize data traffic and improve computation performance through quantitative analysis of multiple design variables, *e.g.*, energy, and latency. Xie *et al.* [325] proposed the DL model construction algorithm and the accelerator for realizing sparse data selection logic on FGPAs, as shown in Figure 30(b). Most of the existing work requires the off-chip DDR memory to store parameters and the expensive DSP module for DL computation on FGPAs. To overcome this issue, Meng *et al.* [326] proposed FixyFGPA, a DL inference accelerator, which supports high sparsity and low precision computation by integrating dense and sparse computation units in FPGAs. Still, it performs poorly in complex computation. Peng *et al.* [333] presents a novel two-position accelerator by

TABLE X: Summary of resource-efficient system software over heterogeneous AIoT devices.

Device type	Technique highlight	Focus level	Resource efficiency improvements	Year	Ref.
MCU	Sparse architecture search, NN-structure pruning	Computation graph	Reduce memory	2019	[226]
	Constraint mapping, NAS	DL model	Reduce memory, reduce latency, reduce energy	2021	[313]
	Matrix multiplication optimization	DL model	Reduce memory,reduce latency	2021	[71]
	Cooperation of NAS and Engine, calculation library optimization	Memory scheduling	Reduce Memory	2020	[12]
	Patch-to-patch inference, optimization of receptive field	Operator	Reduce memory	2021	[123]
ARM	Parallel convolution algorithm based on Fast Fourier transform	Compiler	Reduce memory, reduce latency	2017	[240]
	Data rearrangement, complex matrix multiplication	DL model	Reduce memory, reduce latency	2020	[319]
	Code automatically generates open source library	Compiler	Reduce memory, improve accuracy	2022	[320]
	Adjust data layout, convolution based on Winograd	Intra-device controller	Reduce memory, reduce latency	2021	[321]
	Pipeline strategy, improve data reuse	Computation graph	Reduce memory, reduce latency	2021	[322]
	Fine memory management and data structure design	Memory scheduling	Reduce memory, improve accuracy	2022	[323]
FPGA	Pipeline strategy, scalable accelerator architecture	Computation graph	Reduce latency; reduce energy	2016	[324]
	Simpler sparse data selection logic	Memory scheduling	Improve resource utilization	2018	[203]
	Support high sparsity, low precision calculation	Computation graph	Reduce latency	2021	[325]
	Two-bit convolution accelerator	DL model	Reduce latency	2021	[326]

combining the deep complex network with the binary neural network to speed up inference on FGPAs.

VI. Open Issues and Future Directions

This section discusses existing challenges and potential misleading directions related to resource-efficient AIoT systems and enabling technologies.

A. Cross-level AIoT System

Despite various optimization techniques at a single level, *e.g.*, algorithm, computation graph, compiler, operator, hardware instruction, without considering their cooperation, we discuss the open issues as below.

(i) Cross-level co-design. Prior efforts in cross-level co-design mainly include algorithm-hardware [339]–[341], compiler-hardware [342], [343], and algorithm-system [12], [344], [345] co-design. The algorithm-system co-design is a promising way to address the increasing complexity of DL models for complicated application problems and optimize the runtime execution of those models on AIoT hardware. While the hardware re-design in the first two types is costly for existing AIoT applications and suitable for brand-new construction. Some of the key open issues in cross-level algorithm-system co-design include: First, *Runtime resource-efficient algorithm*. The challenge is how to propagate the feedback of the runtime system execution to the algorithm design. State-of-the-art on algorithm-system co-design like PCONV [346], PatDNN [344], and CoCoPIE [345] simultaneously optimize the model compression algorithms and runtime operator/memory scheduling mechanisms. They leverage some fixed resource-friendly patterns to guide model design. Specifically, DL models are specified with a specific shape to maximize and sustain instruction-level and thread-level parallelism. Second, *Model-adaptive runtime compiler/engine*. Most of the existing works at the compiler and engine level for operator/memory scheduling only manually optimize partial factors. For example, the co-design MCUNet is composed of TinyNAS and TinyEngine. TinyNAS searches for the most efficient model architecture running on TinyEngine. At the same time, the TinyEngine library generates codes for the network search space of TinyNAS to eliminate instruction and memory redundancy. Moreover, it is non-trivial to make the compiler/engine to be compatible with various hardware backends of AIoT devices. They consist of multiple processing units with different architectures and capabilities, *e.g.*, Jetsons [347], Raspberry Pis [144], FPGAs [348].

(ii) Cross-level adaptive controller. Given heterogeneous AIoT devices and diverse performance demands, it is necessary to automate the adaptive optimization control across multiple levels, *e.g.*, DL model, operator, memory allocation, compiler, engine, and hardware instructions. The adaptive controller at the algorithm level with automatic search, *e.g.*, neural architecture search (NAS), is widely explored [349]–[351]. While the adaptive controller across algorithm and system levels is less explored. The challenges are from three aspects: First, the *combined search space* should consider the complex cross-level dependency and collaborations in different techniques, as mentioned in III and IV. Second, the *performance validation* of candidates is non-trivial because the cross-level algorithm and system co-design cover multiple phases, *i.e.*, offline model design and parameter training, runtime compiler, and accuracy testing. Integrating their validation and verification together is desired yet challenging, especially as the design becomes more complex. Third, the *runtime search algorithm*, *i.e.*, boosting the efficiency and efficacy of solving constrained multi-objective optimization problems, is a long-term open problem [352] [353].

B. Context-aware AIoT System Evolution

As discussed in § II-E, to ensure that the deployed AIoT system can maintain continuous and stable high-quality services in the long-term life cycle, the resource demands of the AIoT system should be evolvable. That is, the AIoT system can be compatible with the *dynamic nature of the deployment context* (*e.g.*, the dynamic resource availability, diverse performance

demands) and integrates the adaptation loop to adjust all the system blocks. The AIoT system evolution requirements include *DL model structure scaling* and *weight retraining*. The former is always caused by mismatching between model resource demand and device resource supply, and the latter is usually required by model accuracy degradation in live sensing data. In particular, the evolvable AIoT system may need to deal with the following problems.

(i) Resource availability monitoring. The key resources affecting DL model deployment (*e.g.*, memory budget) and performance outcome (*e.g.*, latency, energy efficiency) in AIoT devices include memory, computing, and battery. All of them exhibit high dynamics over time [8]. For example, the battery-powered device will gradually consume energy as the device runs, and the available memory or computing resources will be encroached upon by other applications/tasks running on a device. The dynamic nature of available resources in AIoT devices is also related to the operating system (OS) resource scheduling. A fast and accurate resource monitor that can interact with heterogeneous and cross-platform OS is needed.

(ii) Resource demand prediction and performance profiling of DL inference/training tasks. The resource demand of deployed AIoT systems contains energy cost, computation, and memory usage. And systematic formulation of these resource demands can predict the most suitable DL inference/training configurations in advance. The AIoT system performance involves DL inference accuracy, inference latency, and training convergence latency. The inference accuracy is coupled with the DNN parameter weights, and dramatic accuracy drop trigger DNN retraining for weight evolving. As mentioned in § II-E, the total computation amount and memory usage for DL inference and training tasks can be directly calculated by the DNN structure and training configurations (*e.g.*, iteration number, batch size). While the prediction of energy demand and latency is non-trivial since its measurement is not straightforward. They heavily depend on the underlying operator scheduling, data flow, and memory bandwidth bound [146]. Measuring energy cost and latency in real-world devices is infeasible or too costly [148]. However, it is highly desirable for many tasks, *e.g.*, searching for the most suitable DNN structure with latency demands from a vast space.

(iii) Dynamic context awareness and system evolution trigger. The dynamic context awareness block detects the mismatch between resource supply and demand or the dramatic accuracy drop to trigger the adaptation block. The triggering station for resource supply-demand mismatch can be further modeled as the noticeable context changes. We note that the onset of the accuracy drop is not always the optimal trigger time point for DNN retraining, which may increase unnecessary retraining workload and even lag some necessary evolution tasks. A suitable trigger is also desired for evolving efficiency and efficacy.

(iv) Automated system loop. The self-evolutionary AIoT system needs an automated loop consisting of the *resource monitor*, the *runtime resource demand and performance profiler*, the *evolution trigger*, and the *optimizer*. The resource monitor tracks the memory/computing resource supply of the available AIoT devices. The resource demand profiler predicts the DL inference tasks' memory, computing, and energy resource demands with the current configurations. If the resource demand exceeds the supply or the accuracy drop exceeds a pre-defined threshold, the evolution trigger notifies the optimizer, adjusting the DL inference/training configurations. The automated control loop routinely checks for system changes and performs on-demand evolution.

C. Distributed AIoT Resource Aggregation in DL inference/training Tasks

Efficiently aggregating memory and computing resources within the networked AIoT system for seamless communication and the provision of complex services is an active and research-intensive domain, which has several open issues.

- How to uniformly manage heterogeneous resources (*e.g.*, SRAM, DRAM, CPU/GPU, battery) within the networked AIoT system? They should be organized and managed in a unified manner to enable efficient DNN training or inference tasks.
- How to combine operator scheduling, memory allocation, and hardware instruction mechanisms within the networked AIoT system. Specifically, the computing power of AIoT devices is subject to the *barrel effect* of memory, computing, and battery resources. The shortest board of the barrel restricts the overall computing capability. Thus, monitoring the AIoT device resources with *normalized assessment necessary* is necessary.
- How to balance multiple performance goals in the resource aggregation process (*e.g.*, energy efficiency and latency)? We need to establish the hierarchical dependence between several internal factors (*e.g.*, DL model, operator, memory, instructions) of the AIoT system and the external environment (*e.g.*, input).
- How to develop hybrid distributed resource aggregation methods that combine both synchronous and asynchronous communication schemes to balance the trade-off between convergence speed and system stability.
- How to deal with the opportunistic connection problem of AIoT devices for guaranteeing resource availability?

Advanced research in areas such as edge intelligence [354] and federated learning [106] intersects with some of the issues mentioned above, but it cannot comprehensively address them. To tackle these challenges, it is important to decouple resource aggregation methods from the DL inference/training tasks and develop them as a general-purpose middleware function that can actively perceive, analyze, and select AIoT resources to meet diverse demands.

D. Intelligence Enhancement in Distributed DL Training

AIoT devices have been extensively deployed in numerous domains. Their wide array of sensors allows for the collection of massive amounts of data, facilitating the execution of DL tasks and enabling different intelligent applications. In practical AIoT systems, a large number of distributed devices continuously sense the environment and hold accumulated datasets. However, real-world scenarios present several challenges that must be addressed to ensure reliable and efficient

data transmission, synchronization, and coordination among these devices. These challenges include:

(i) Intrinsic linkages of distributed holding datasets.. To fully leverage the distributed devices' computing power and accumulated datasets, studying the intrinsic linkages between distributed datasets in different AIoT sub-clusters and designing corresponding distributed DL training systems is essential. In particular, the inherent correlation, redundancy, and hysteresis of distributed datasets can drive the design of distributed training systems, leading to high-quality, responsive, and low-cost distributed DL training.

(ii) Temporal collaboration of distributed devices. In real-world AIoT systems, each device may have different training power and speed. Asynchronous communication methods have been proposed to mitigate this problem to some extent [355], but extreme temporal differences still pose a significant challenge to participant collaboration. Specifically, the challenge is effectively promoting collaboration among participant devices with different temporal patterns. For example, existing distributed DL training systems often partition the dataset by data category to highlight the Non-IID nature of the data [356]. However, the data distribution collected by AIoT devices is clearly more diverse and challenging. Possible directions for distributed DL training can consider:

- The temporal correlation of the distributed data at diverse sub-clusters of AIoT devices varies. Distributed DL model/data aggregation and communication mechanisms in AIoT system's distributed learning for syn-/asynchronic datasets/models should be different.
- The spatial correlation of the distributed data in distributed DNN training, *e.g.*, physically nearby devices have the potential for better collaboration gains.
- We can divide the participating AIoT devices into diverse roles in distributed DL training, *e.g.*, collaborators, competitors, and supervisors.

E. Inference and Training Task Balance in Resource-constrained AIoT Devices

Resouce-constrained AIoT devices always load lightweight Dl models, such as compressed DL models. However, DL models with shallow or sparse structures are highly susceptible to data drift, which occurs when the live data stream captured by the devices diverges from the data used for training, leading to a drop in accuracy in real-world applications. Some efforts [357]–[359] have proven that DL models deployed in AIoT devices should be continuously retrained using newly captured live data to maintain accuracy.

However, AIoT devices provide limited resources to execute computation. Introducing training tasks into AIoT devices will likely *deprive resources of the inference tasks for training*, leading to decreased inference performance. The more resources we allocate to the task of DL retraining, the faster the training process will be, and we can obtain a high-accuracy inference model earlier. However, the limited resources allocated to the inference task during the training process may decrease the overall performance of DL inference. On the other hand, allocating too few resources to the retraining task may slow down the retraining speed and delay the accuracy improvement of the updated model, which could impact the timely inference accuracy gain. Therefore, it is crucial to trade off the accuracy improvement from training with real-time inference performance. We discuss open issues in more detail:

- How to allocate resources for maximizing the inference accuracy when the training task deprives a certain amount of memory, regarding the tunable data flow in memory units. For example, we can share memory resources between the inference and training tasks via memory reallocation, recomputation, and swapping techniques.
- How to select promising DL training tasks and allocate computing resources among them in AIoT devices.
- How to select DL training configurations (*e.g.*, epoch) and inference configurations (*e.g.*, sampling rate) to maximize inference accuracy with minimum resource usage.

Making accurate decisions on resource allocation and performance assessment is challenging in advance DL training. Furthermore, due to the dynamic nature of AIoT context, the optimal resources and configurations may change over time. The best decision at the current training may become sub-optimal for future training phases.

F. Memory-computation Feedback and Joint-optimization

Memory and computation cost of DL models are two crucial metrics tunable in AIoT systems to affect overall performance, *e.g.*, delay, and energy cost. However, previous studies have shown that memory and computation optimization are often conflicting goals. For instance, recomputation techniques can save memory space by discarding and recalculating intermediate activations, but they can also introduce extra computing delay [120], [121], [223]. Further research is needed to balance these two metrics best and enable memory-computation joint optimization in AIoT systems.

(i) Near- and in-memory computing. The underlying memory schedule techniques have not kept up with computation optimization advances in latency and energy reduction over the years, referred to as the memory wall [360]. The development of DL has exacerbated this problem as the frequent movement of a large amount of data, including input data and intermediate activations between memory and compute units. They seriously impacted the latency and energy cost of DL training and inference tasks. To address this issue, some studies [361]–[365] physically relocate compute units (multi-core, GPU, FPGA) closer to memory to reduce data transport costs. Near-memory and in-memory computing embed computation in the memory array. As compute units become more intimately connected with memory, finer-grained parallelism can be proposed to improve energy efficiency and latency [366]–[369]. However, these compute units placed next to memory have problems such as less supporting computing types and weak computing power. Thus, designing at the system level, rather than the hardware level, to deploy data-intensive operators (such as ReLU) in near-memory compute units is promising, especially for ubiquitous AIoT devices without hardware replacement. DL operators need to access a large amount of data for computing, which causes considerable

data transfer delay and lower computing demands. Also, we can carefully allocate DL operators to the near- and in-memory units to reduce memory access costs and improve computation efficiency at the operator and instructor levels.

(ii) Memory-aware computing in runtime/compiler optimization. Memory-computation joint optimization for AIoT can be achieved by co-designing the DL algorithm and engine. At the algorithm level, we can interleave computation-intensive and data-intensive operators to balance the workload of compute units near memory. At the engine level, we can optimize the computation graph and generate execution code to reduce access delay for data-intensive operators. These can be achieved by optimizing the inner layers of the loop.

VII. Conclusion

Artificial Intelligence of Things (AIoT) combines AI technologies with IoT infrastructures, enhancing the efficiency and efficacy of data analysis. However, due to the heterogeneous and dynamic nature of AIoT hardware, co-designed cross-level AIoT system and adaptive controllers are needed to expand the boundaries of system performance beyond what can be achieved by algorithm-level techniques alone. These co-designed systems can push the boundaries of resource-performance tradeoffs for AIoT. Specifically, the cross-level AIoT system spans on-device and distributed DL training/inference algorithms, computation graphs, operators, memory schedules, hardware instructions, *etc.* With the continuous development of DL technologies and AIoT devices, the AIoT system expands the cyber-physical space to the human space, providing low-cost, high-quality, and inclusive ubiquitous intelligence for a wide range of AIoT application domains. Given the heterogeneous and dynamic nature of AIoT hardware, co-designed cross-level AIoT systems, and adaptive controllers can further expand the boundaries of system performance, including accuracy and resource consumption, beyond what can be achieved with algorithm-level or system-level techniques alone. We hope this survey will raise awareness and stimulate discussion among researchers and developers on AIoT system. This paper elucidates many aspects of distributed device collaboration (*i.e.*, network topology establishment), and data exchange in real-world inference and training tasks. These insights are invaluable for communication researchers, as they provide a deeper understanding of the intricacies involved. More heuristics and insights are needed to ensure resource-efficient AIoT systems. For example, reliable and real-time communication can further enhance network efficiency in AIoT deployments.

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